APPENDIX VI
(to Recommendation G.961)

Basic access transmission system using SU32 line code

VI.0 *General*

The SU32 standard will support the full duplex, transparent transmission of two 64 kbit/s B channels and one 16 kbit/s D channel over symmetric pair cables using echo cancelling techniques. In addition to transparent 2B + D transmission, 5.3 kbit/s capacity is provided for an Auxiliary channel supporting data CRC, control, supervisory and maintenance functions. The bit stream is encoded for transmision using a high performance ternary SU32 (substitutional 3B2T) conditional block code, filtered and transmitted to line at a baud rate of 108 kbauds. An orthogonal timing signal is superimposed on the line code for symbol sampling; which does not compromise either the line code efficiency or performance. A unique synchronisation word is used to achieve frame synchronisation. Fast and reliable activation is ensured by means of a binary handshake procedure, for separate training of canceller and equaliser.

VI.1 *Line code*

The binary data is encoded into a ternary form using the SU32 line code. This is based on the fixed and unconditional 3B2T line code and modified as follows. Each binary triplet is converted to a ternary duplet and is transmitted unless it is identical to the previously transmitted duplet. If current and previous duplets are identical, then the un-used code word ‘‘00’’ is transmitted in its place. The SU32 coding rule is shown in Table VI-1/G.961. In this Table, the left most bit is the first into the encoder and the left most symbol the first out of the encoder.

H.T. [T35.961]
TABLE VI-1/G.961
SU32 coding (substitutional 3B2T)

Binary I/P	Ternary O/P	Binary I/P	Ternary O/P
000	——	100	0—
001	—0	101	+—
010	—+	110	+0
011	0+	111	++

Tableau VI-1/G.961 [T35.961], p.

Decoding

Decoding of the received signal is the inverse of the coding process.

Tolerance to line polarity inversion

The code is symmetric so that inversion of the ternary data results in an inversion of the decoded binary data. Thus polarity correction due to cable inversion can be applied either to scrambled or unscrambled binary data, or to ternary data. Both transmitted and received polarity correction is performed at the NT1.

VI.2 *Symbol rate*

The symbol rate is determined by the line code, the bit rate of the information stream and the frame structure. The symbol rate is 108 kbauds.

VI.2.1 *Clock tolerance*

VI.2.1.1 *NT1 free running clock accuracy*

The tolerance of the NT free running clock shall be ± | 92 ppm.

VI.2.1.2 *Tolerance of the free running clock in the LT*

The free running clock in the LT will be phase locked to the exchange clock having a frequency tolerance of ± | 0 ppm thus permitting operation with any equipment meeting Recommendation G.703.

VI.3 *Frame structure*

There are two states of operation of the transmission system, steady state and training state. The frame structure covered in this section is for the steady state (information transfer).

The B1, B2, D and CL channels map directly from binary bits through the scrambler into the ternary frame structure. The SU32 code table is designed to exclude certain uniquely identifiable code sequences, which are exploited for synchronisation purposes.

Multiframe: Multiframe word and location

The 12 ms multiframe is identified every 16th 3/4 ms frame by replacing the CRC data symbol (No. 79) with a ternary ‘‘0’’. In all other frames, this symbol is binary valued. This, combined with the frame synchronisation word preceding it, uniquely identifies the position of the start of the superframe.

Multiframe Format

A multiframe consists of sixteen 81-ternary-symbol 0.75 ms frames.

6 frames of 2B + D Frame word CRC_1 $CL\text{-}channel_1$ 6 frames of 2B + D Frame word CRC_2 $CL\text{-}channel_2$ 6 frames of 2B + D Frame word CRC_3 $CL\text{-}channel_3$

6 frames of 2B + D Frame word CRC_4 $CL\text{-}channel_4$ 6 frames of 2B + D Frame word CRC_5 $CL\text{-}channel_5$ 6 frames of 2B + D Frame word CRC_6 $CL\text{-}channel_6$

6 frames of 2B + D Frame word CRC_7 $CL\text{-}channel_7$ 6 frames of 2B + D Frame word CRC_8 $CL\text{-}channel_8$ 6 frames of 2B + D Frame word CRC_9 $CL\text{-}channel_1$

6 frames of 2B + D Frame word $CRC_{1\backslash d0}$ $CL\text{-}channel_2$ 6 frames of 2B + D Frame word $CRC_{1\backslash d1}$ $CL\text{-}channel_3$ 6 frames of 2B + D Frame word $CRC_{1\backslash d2}$ $CL\text{-}channel_4$

6 frames of 2B + D Frame word $CRC_{1\backslash d3}$ $CL\text{-}channel_5$ 6 frames of 2B + D Frame word $CRC_{1\backslash d4}$ $CL\text{-}channel_6$ 6 frames of 2B + D Frame word $CRC_{1\backslash d5}$ $CL\text{-}channel_7$ 6 frames of 2B + D Frame word ‘‘0’’ $CL\text{-}channel_8$

1 72, 73 . | | 78 . | | 79 . | | 80 81 <-------------------- 750 μ sec transmission frame --------------------> **12 ms multiframe structure** *Note* — B1, B2, D and CL channel data is scrambled. CRC data and frame words are not scrambled.

VI.3.1 *Frame length*

There are 6 (2B + D) slots in each 3/4 ms 81 symbol frame.

VI.3.2 *Binary bit allocation in direction LT to NT*

The following binary bit ordering is applied before scrambling.

H.T. [T36.961]

B1 1	B1 2	B1 3	B1 4	B1 4	B1 5	B1 6	B1 7	B1 8	B2 1	B2 2	B2 3	B2 4	B2 5	B2 6	B2 7	B2 8	D 1	D 2
B1 1	B1 2	B1 3	B1 4	B1 4	B1 5	B1 6	B1 7	B1 8	B2 1	B2 2	B2 3	B2 4	B2 5	B2 6	B2 7	B2 8	D 1	D 2
B1 1	B1 2	B1 3	B1 4	B1 4	B1 5	B1 6	B1 7	B1 8	B2 1	B2 2	B2 3	B2 4	B2 5	B2 6	B2 7	B2 8	D 1	D 2
B1 1	B1 2	B1 3	B1 4	B1 4	B1 5	B1 6	B1 7	B1 8	B2 1	B2 2	B2 3	B2 4	B2 5	B2 6	B2 7	B2 8	D 1	D 2
B1 1	B1 2	B1 3	B1 4	B1 4	B1 5	B1 6	B1 7	B1 8	B2 1	B2 2	B2 3	B2 4	B2 5	B2 6	B2 7	B2 8	D 1	D 2
B1 1	B1 2	B1 3	B1 4	B1 4	B1 5	B1 6	B1 7	B1 8	B2 1	B2 2	B2 3	B2 4	B2 5	B2 6	B2 7	B2 8	D 1	D 2

Tableau [T36.961], p.

The binary data is scrambled as defined in § VI.9 and ternary encoded. It is then multiplexed into the following frame format.

H.T. [T37.961]

T 1	T 2	T 3	T 4	T 5	T 6	T 7	T 8	T 9	T 10	T 11	T 12
T 13	T 14	T 15	T 16	T 17	T 18	T 19	T 20	T 21	T 22	T 23	T 24
T 25	T 26	T 27	T 28	T 29	T 30	T 31	T 32	T 33	T 34	T 35	T 36
T 37	T 38	T 39	T 40	T 41	T 42	T 43	T 44	T 45	T 46	T 47	T 48
T 49	T 50	T 51	T 52	T 53	T 54	T 55	T 56	T 57	T 58	T 59	T 60
T 61	T 62	T 63	T 64	T 65	T 66	T 67	T 68	T 69	T 70	T 71	T 72

Tableau [T37.961], p.

VI.3.3 *Binary bit allocation in direction NT1 to LT*

The frame structure and order of bits in the NT1 to LT direction is to identical that used in the LT to NT1 direction specified in § VI.3.2 above.

VI.4 *Frame word*

The frame word of six ternary zeros terminated by the binary CRC$_{1\backslash d5}$bit (as illustrated in the above Table) is used to define the 0.75 ms frame boundaries. Note that once every superframe a ternary zero is substituted for the binary CRC check bit. This frame word is unique and cannot be emulated by any 2B + D data pattern.

The frame word specified above is the same in both directions of transmission.

VI.5 *Frame alignment procedure*

The frame alignment function is specified in the Activation sequence. 2B + D transmission cannot commence unless frame alignment has been achieved. Initial frame alignment is considered to have been achieved when the cumulative total of correct versus incorrectly received 7-bit frame words exceeds 4. In steady state operation, this cumulative count is maintained but limited to a maximum of 64. Frame alignment loss is flagged if this cumulative total falls below two.

VI.6 *Multiframe*

The multiframe structure has been described in the frame structure, § VI.3 of this Appendix.

VI.7 *Frame offset between LT-NT1 and NT1-LT frames*

No specific phase requirements are necessary between frames in the LT-NT1 and NT1-LT directions.

VI.8 *CL channel*

An embedded protected operations channel (EPOC) of 4 kbit/s is partially allocated to supervisory and maintenance functions. Significant spare capacity and undefined bits remain for both future allocation of messages as well as specific national requirements.

This channel is protected by a 6-bit CRC check and compelled protocol which provides that all messages are repeated every 6 ms.

VI.8.1 *Bit rate*

Twenty-four bits per 6 ms multiframe (4 kbit/s) are allocated to an embedded protected operations channel (EPOC). This supports supervisory and maintenance functions between the network and the NT1 and includes spare capacity for user defined functions. Additionally a further 1.33 kbit/s is allocated to provide an error detecting CRC15 and 12 ms framing to the CL channel.

VI.8.2 *Structure*

Within each 12 frame, the operations channel sends two consecutive messages of 24 bits. Each 24 bit message comprises:

— 1 bit Ready for data/data valid (R).

— 5-bit Maintenance channel (M).

— 9-bit Supervisory channel (S).

— 3 Unassigned bits (500 bit/s subsidiary channel).

— 6-bit Cyclic redundancy check field (CRC).

The structure of the CL channel is as follows:

H.T. [T38.961]

Unable to convert table

Tableau [T38.961], p.3

VI.8.2.1 *Maintenance messages*

In the ET to NT1 direction 9 of the 32 possible command messages are allocated. An identical message is returned in the NT1 to ET direction as an acknowledgement.

ET to NT1 maintenance message codes No. Message 5-bit code M1 M2 M3 M4 M5

1 No loopback (null message)/remove loopback 1 1 1 1 1 2 Provide loopback B1 at NT1 1 1 0 1 1

3 Provide loopback B2 at NT1 1 0 1 1 1 4 Provide loopback B1 + B2 at NT1 1 0 0 1 1

5 Provide loopback B1 + B2 + D at NT1 1 0 0 0 1 6 Provide loopback B1 at regenerator 0 0 1 1 1

7 Provide loopback B2 at regenerator 0 1 0 1 1 8 Provide loopback B1 + B2 at regenerator 0 1 1 1 1

9 Provide loopback B1 + B2 + D loopback at regenerator 0 1 1 0 1

Supervisory sub-channel message formats

A 9-bit field is available in each direction of transmission to allow supervisory information to be provided. This contains an 8-bit data/address field and a one-bit flag used to indicate whether or not the 8-bit field contains valid data.

ET to NT1 supervisory message command codes

No Supervisory message and destination S-interface 1 No supervisory information requested 1 1111 1111 2 ET AGC value 0 0000 0100 3 ET eye closure 0 0000 0101

4 ET eye height 0 0000 0110 5 ET CRC error count 0 0000 0111 6 NT1 AGC value 0 0001 0000 7 NT1 Eye closure 0 0001 0001

8 NT1 Eye height 0 0001 0010 9 NT1 CRC error count 0 0001 0011 11 Regenerator LT-side receiver AGC 0 0000 1000 12 Regenerator LT-side receiver Eye closure 0 0000 1001

13 Regenerator LT-side receiver Eye height 0 0000 1010 14 Regenerator LT-side receiver CRC count 0 0000 1011 15 Regenerator NT1-side receiver AGC 0 0000 1100 16 Regenerator NT1-side receiver Eye closure 0 0000 1101

17 Regenerator NT1-side receiver Eye height 0 0000 1110 18 Regenerator NT1-side CRC count 0 0000 1111

VI.8.3 *Protocols and procedures*

The maintenance channel is used to set loop backs from the LT. When a maintenance message has been received free from error and implemented, the same message is echoed back from the NT1 to the LT.

The supervisory channel is designed to be used as a compelled system, with a command sent by the LT end until the expected response is received. A delimiting idle message of nine ONEs is employed. All valid messages and responses set the first bit of the 9 supervisory bits to a ONE. An 8 bit word can therefore be securely passed across this channel. An example use of the supervision channel is for reporting eye closure information from the NT1 to the LT.

VI.8.4 *CL channel performance*

With a mean 144 kbit/s error rate of 1 in 1000, characterised by a mean error burst size of 10, the following performance will be achieved:

a) 99.8% of all messages will be conveyed within 6 ms.

b) No more than one message per hour shall be conveyed in more than 18 ms.

c) The mean erroneous error message rate is less than one per hour with a maximum time to correction of 18 ms.

VI.9 *Scrambling*

B1, B2, D and C channel binary data is scrambled as follows:

a) NT to LT scrambler polynomial

$$1 \oplus x^{-18} \oplus x^{-23}$$

(where $\oplus$ denotes exclusive OR)

b) LT to NT scrambler polynomial

$$1 \oplus x^{-5} \oplus x^{-23}$$

VI.10 *Activation/deactivation*

VI.10.1 *Signals used for activation*

Figure VI-1/G.961 illustrates the activation sequence initiated by the ET in terms of function elements (FE) and INFO's.

Figure VI-2/G.961 illustrates the activation sequence initiated by the user in terms of function elements (FE) and INFO's.

Figure VI-1/G.961, (N), p.4

Figure VI-2/G.961, (N), p.5

The definition of the function elements, LT states and NT states used in the activation Figures and the state transition tables in this Appendix is as follows.

Definition of FE's LT's and NT's Function elements (FE) FE1 Activation request for the interface from the ET. FE2 Line signal detected on the digital section.

FE3 The digital section is activated (in synchronisation). FE4 The user network at the T reference point is activated or a loopback is operated. FE5 Deactivation request for the digital section. FE6 The digital section and the interface at the T reference point has been de-activated. FE7 Error indication. (Loss of synchronisation or no line signal detect).

NT1 states NT1 The NT1 is ready for activation. NT2 The NT1 is executing the digital section training sequence. NT3 The NT1 is in synchronisation with the LT and the LT to NT1 digital section is capable of error free data transmission. NT4 Equivalent to state NT3 plus synchronisation of the interface at the T-reference point.

NT5 The 2B + D data channel through the digital section and across the T reference point is fully operational. NT6 The NT1 has sent an activate request to the LT and is waiting for a response. NT7 The NT1 is not active but is not ready for activation.

LT states LT1 The LT is ready for activation. LT2 The LT is executing the digital section training sequence. LT3 The digital section has been correctly activated and is synchronised in both directions. LT4 Both the digital section and the interface at the T reference point are correctly activated and synchronised.

LT5 The 2B + D data channel through the digital section and across the T reference point is fully operational. LT7 The LT has ceased transmission over the digital section and is waiting for all line signals to disappear.

The response of the digital section to the activation request FE1 from the ET or the activation request INFO 1 from the TE is to signal across the digital section by the transmission of a quarter baud rate (27 kHz) wake-up tone.

In the NT1 to LT direction, the duration of this wake up tone shall not be less than 32 complete cycles of the repetitive data pattern +--+. The tone shall not exceed 10 ms in duration.

In the LT to NT1 direction, the duration of the wake-up tone shall not be less than 32 complete cycles of the repetitive data pattern +--+. The tone shall not exceed 10 ms in duration.

VI.10.2 *Definition of internal timers*

The activation procedure shall nominally take 120 ms to the point where error free framed transmission can commence.

In the event of the activation procedure failing, or loss of synchronisation on either the interface at the T-Reference point or on the transmission system described herein, a timer is required in the NT to terminate operation. This timer shall not exceed 65 ms measured from the point of loss of synchronisation; or in the case of activation, measured from the time at which synchronisation should be achieved.

It is not essential to employ a timer for the identification of failure to activate or loss of synchronisation signalled to the LT. However, where there is no external control of the de-activation procedure applied to the two wire LT termination, a timer not exceeding 65 ms from the time of loss of synchronisation or as measured from the time at which activation should have been achieved should be employed.

VI.10.3 *Activation procedure*

Table VI-2/G.961 shows the training sequence signals that should be transmitted to line by the LT and NT1. At the LT, offsets are measured in baud periods from the end of the wake-up tone transmission. At the NT1, offsets are measured in baud periods from the detection of the end of the wake-up tone. For correct operation, it is necessary that the time from the LT completing the wake-up tone burst, to the NT1 detecting the end of wake-up tone is less than or equal to 32 bauds.

H.T. [T39.961]

TABLE VI-2/G.961

Activation training sequence

Offset (bauds)	Duration (bauds)	LT timing signal	LT data	NT timing signal	NT data
| 0	64	OFF	None	OFF	None
| 64	512	ON	None	OFF	None
| 76	512	OFF	None	ON	None
1 | 88	512	ON	None	OFF	None
1 | 00	512	OFF	None	ON	None
2 | 12	4096	ON	PRBS	OFF	None
6 | 08	32	ON	None	OFF	None
6 | 40	4064	ON	None	OFF	PRBS
10 | 04	(405) (Note 1)	ON	Ternary (Note 1)	OFF	None
10 | 09 (Note 1)	(405) (Note 2)	ON	Ternary (Note 2)	OFF	Ternary (Note 2)

PRBS stand for a 511 bit pseudo-random binary sequence generated by the polynomial (1 $\oplus x$ $^{\mathrm{D}}$lF261^{4} $\oplus x$ $^{\mathrm{D}}$lF261^{9}).

Note 1 — The transmission of ternary data from the LT to the NT1 from this time onwards in continuous. The NT1 will not return ternary data until it has achieved synchronisation, the figure of 405 bauds and the subsequent offset to the next row is intended as a guide to the normal duration for this process.

Note 2 — Ternary transmission from NT1 to LT implies that error-free transmission and frame synchronisation have been achieved in the NT. Following the LT acquiring synchronisation, full duplex 2B | | transmission can commence.

Tableau VI-2/G.961 [T39.961], p

The conditional step between the NT1 acquiring synchronisation and returning ternary data is included to provide a mechanism by which the optional alignment of LT to NT1 and NT1 to LT frame words can be achieved.

VI.10.4 *State transition table of the NT*

See Table VI-3/G.961.

H.T. [T40.961]

TABLE VI-3/G.961

State transition table of the NT

	State	NT1 ready for act.	NT2 training	NT3 wait for T	NT4 wait for data valid	NT5 steady state	NT6 TE act.	NT7 pending deact.
	Signal transmitted to TE	I0	I0	I2	I2	I4	I0	
Events								
Source	Event							
LT	Activate indication [FE1]	NT2	—	—	—	—	NT2	—
NT1	In synch. [FE3]	/	NT3	—	—	—	/	—
TE	INFO 3	/	/	NT4	—	—	/	—
NT1	Data valid	/	/	/	NT5	—	/	—
TE	Activate indication INFO 1	NT6	/	/	/	/	/	—
NT1	Loss of synch. [FE3]	—	NT7	NT7	NT7	NT7	—	—
NT1	No line sig. detect on DS	—	—	—	—	—	—	NT1

— No change

/ Impossible

[ ] Remote source event

DS Digital system

Tableau VI-3/G.961 [T40.961], p.

VI.10.5 *State transition table of the LT*

See Table VI-4/G.961.

H.T. [T41.961]

TABLE VI-4/G.961

State transition table of the LT

	State	**LT1 Ready for act.**	**LT2 Training**	**LT3 Dig. sect. active**	**LT4 T-ref in synch.**	**LT5 Steady state**	**LT7 Pending deact.**	
	Signal transmitted to DS	**Inactive**	**Training seq.**	**Steady state**	**Steady state**	**Steady state**	**Inactive**	
Events								
Source **ET** **(activate reqst.)**	**Event** **FE1**	**LT2**	**/**	**/**	**/**	**/**		**—**
LT	**DS in-synch.**	**/**	**FE3 LT3**	**—**	**—**	**—**		**/**
LT **No line activity** **LSD > False**	**FE2**	**/** **—**	**—**	**—**	**—**		**LT1**	
NT1 **Ready for data**	**[INFO 3]**	**/**	**/** **LT4**	**FE4**	**—**	**—**		**/**
LT **DS loss of synchronisation**	**/**	**LT7**	**FE7** **LT7**	**FE7** **LT7**	**FE7** **LT7**	**FE7**	**—**	
ET **deactivation request**	**FE5** **/**	**LT7**	**FE7** **LT7**	**FE7** **LT7**	**FE7** **LT7**	**FE7**	**—**	
ET Data valid	**/**	**/**	**/**	**LT5**	**—**		**—**	

— No change

/ Impossible

[| Remote source event

LSD Line signal detect

Tableau VI-4/G.961 [T41.961], p.

VI.10.6 *Activation times*

The ‘‘cold start’’ and ‘‘warm start’’ times will be 120 ms± | 0 ms with all cable combinations permissible. This reliable and repeatable activation time is a result of the specific activation sequence specified in this SU32 standard.

VI.11 *Jitter*

Jitter performance must be sufficient for the purpose of providing the clock for interface at the T-reference point transmission function in accordance with Recommendation I.430.

The SU32 proposal features an orthogonal timing signal superimposed on the data. This leads to stable and low jitter digital phase locked loop timing circuitry being easily achieved.

VI.11.1 to V1.11.3

For further study.

VI.12 *Transmitter output characteristic of the NT or LT*

VI.12.1 *Pulse amplitude*

The nominal pulse amplitude shall be zero to peak 1.8 volts. The tolerance on this peak pulse amplitude shall be such that signal power and amplitude vs. frequency spectrum performance is as specified in § VI.12.

VI.12.2 *Pulse shape*

The pulse shape is determined by the pulse mask of Figure VI-3/G.961.

Figure VI-3/G.961, (N), p.

VI.12.4 *Power spectrum*

SU32 has a code spectrum modified by the conditional coding rule compared to random ternary signalling. The theoretical power spectrum when using SU32 having full width rectangular pulse shaping with transformer coupling is given in Figure VI-4/G.961.

Limits for the transmitted power spectral density are given in Figure VI-5/G.961.

Figure VI-4/G.961, (N), p.10

Figure VI-5/G.961, (N), p.11

Power levels

Signals sent to line must conform to the following criteria, under all operating conditions with 140 ohms resistive termination:

a) The maximum total transmit power, averaged in any 1 second period must not exceed +11 dBm.

b) The maximum transmit power average in any 1 second period in any 3 kHz band, below 100 kHz, must be less than 0 dBm. This limit extends down to DC (excluding power feed).

c) The nominal recommended transmit power will be +9.5 dBm with a tolerance of ± | dB.

VI.13 *Transmitter/receiver termination*

VI.13.1 *Impedance*

The nominal output/input impedance looking towards the NT shall be 140 ohms. The nominal output/input impedance looking towards the LT shall be 140 ohms.

VI.13.2 *Return loss*

For further study.

VI.13.3 *Longitudinal conversion loss*

The longitudinal conversion loss in the range 100 Hz to 1.6 times the symbol rate (fO) shall exceed 46 dB. For a frequency 10 MHz > f > 1.6 f_0, the longitudinal loss shall exceed 46 — 40 log (f/1.6 f_0) dB or 24 dB whichever is greater.

Supplement No. 15

ALMOST-DIFFERENTIAL QUASI-TERNARY CODE (ADQ CODE)

(Referred to in Recommendation G.911, this Supplement is to be found on page 673

of Fascicle III.3 of the Orange Book, Geneva, 1977)

Supplement No. 27

INTERFERENCE FROM EXTERNAL SOURCES

(Referred to in Recommendations G.221 and G.950; this Supplement is to be found on page 346 of Fascicle III.2 or on page 390 of Fascicle III.3 of the Red Book, Geneva, 1985.)

Supplement No. 34

TEMPERATURE IN UNDERGROUND CONTAINERS FOR THE INSTALLATION | OF REPEATERS

(Melbourne, 1988)

(see Recommendation G.950)

1 General

This Supplement consists of two parts: A and B.

Part A | (source: Federal Republic of Germany) informs about the ground temperature taken from meteorological sources in most regions of the world, and shows the seasonal variations as a function of the depth (in the Federal Republic of Germany).

Part B | (source: Italy) gives guidelines for the calculation of the ground temperature in the container, depending, *inter alia* , from the atmospheric temperature, the depth and the dissipation of the equipment in the container.

Both parts give additionally some general information which is useful as a guidance for planning.

2 Part A

2.1 *Definition*

In the following, climatic conditions are discussed which are relevant to small underground containers without any means for adjusting to specific temperature conditions. These containers are normally hermetically closed and need not be opened e.g., for preventive maintenance. They can be operated with or without gas pressure supervision or they may contain drying agents.

2.2 *Temperature in underground containers*

The temperature in underground containers depends on the temperature of the surrounding soil. Additionally, it is influenced by the power dissipation of the installed equipment.

The ground temperature at various depths is well known for most of the regions of the world [1]. Figure 1 shows the seasonal variation of the ground temperature as a function of the long term mean value of the ground temperature. Examples of the variation of the temperature with time for a period of 1 year is shown in Figure 2. The yearly minimum and maximum temperatures as a function of the depth are plotted in Figure 3. Figures 2 and 3 are examples only for a specific region in Germany (Federal Republic of) and for sandy soil.

Figure 1, (N), p.12

Figure 2, (N), p.13

Figure 3, (N), p.14

The composition of the soil has a significant effect on the temperature and its variation with time. It should be noted that this variation occurs slowly, depending on the composition of the soil and on the depth.

The mean value of the temperature in the container is the same as that of the ground, if the possible increase caused by the heat generated by the power dissipation of the equipment is neglected. Variations of the air temperature cause variations of the temperature in the container, but with a time delay, and with an attenuation of the amplitude depending on the design of the container.

2.3 *Conclusion*

The temperature in small underground containers e.g., for the installation of remote power-fed repeaters depends on the geographical region, the composition of the soil, the depth of installation and the power dissipation of the installed equipment.

The humidity within the container is independent of external influences and can be controlled by suitable means, if necessary.

3 Part B

3.1 *Temperature in underground housing containing high dissipation equipment*

The temperature in the underground housing depends on the temperature of the surrounding soil, its composition and on the amount of power dissipated in the equipment.

3.1.1 The temperature in the soil at different depths can be directly measured at the site or can be calculated from seasonal mean temperature of the site (at ground level) taking into account thermal resistivity and diffusity of the soil.

Short term variations, like daily excursions, are rapidly damped and become negligible at a depth greater than 0.3 m so that only seasonal variation diffuses farther in the ground.

Of course such variations too are attenuated and delayed following the depth and the soil composition.

3.1.2 The heat generated by equipment dissipation in the housing is transferred via housing walls into surrounding soil thus disturbing the existing temperature field and determining a local gradient which decreases with the distance from housing walls.

In order to evaluate the maximum annual temperature in the housing it is advisable to define a mathematical model of the heat transmission and solve it for the conditions imposed by the site climate, the soil nature, the power consumption, etc.

The relevant calculation can be handled by computer making it possible to rapidly investigate the effect of the different parameters.

In critical condition, that is in soil of poor characteristics, advantage can be taken putting around the housing a backfilling material of good thermal conductivity. The effect of such an action can be previously verified by computer.

3.2 *Guidelines of the calculus*

The heat transmission from the atmosphere to the soil is described by the equation

where

- A Mean value of the atmospheric temperature
- B Amplitude of the thermal oscillation at the ground surface
- γ Coefficient of diffusion
- y Depth

The temperature is a function of the time and depth only and the resulting field has horizontal isothermal surfaces.

The power dissipated in the housing determines a heat flux on the walls of the container and a two-dimensional thermal field in the soil.

The relevant equation is the

where

$F(x, y, t)$ takes into account the presence of thermal sources in the soil

C Specific heat of the soil

ζ Density of the soil

k Thermal conductivity of the soil.

The problem can be further simplified neglecting the term $\frac{(*\mathrm{d}T}{(*dt}$.

In fact the temperature in the soil is subjected to a slow variation and can be considered as steady in the short period.

Solve the equation

and introducing the ‘‘initial condition’’ of the (1) for the considered time, the temperature distribution in the soil can be plotted in a discrete number of points.

The centreline temperature in the housing is calculated from heat transfer relationships for natural convection on vertical walls: Nu = M. (G r | (mu | r)^N where NU = Nusselt number; GR = Grashof number; Pr = Prandtl number; M, N are constants to be empirically determined.

An example of calculated thermal field is given in Figure 4 where the isothermal lines substitute the local temperature values plotted by computer.

Figure 4, (N), p.

3.3 *Conclusion*

The temperature in the underground housing depends on site climate, type of soil, depth, time of the year, equipment dissipation.

A mathematical analysis of the heat transmission makes it possible to evaluate the maximum temperature in the housing taking into account the effect of the parameters involved.

The use of selected backfilling material can be considered and the resulting effect evaluated.

HOUSING TYPE : CAI/24

Temperature at steady state (° |)

Housing dimensions (m) ∅ 0.85 h 0.9

Dissipated power (watt)	100
Month	8
Mean temperature of the site (° |)	12.7
Amplitude of the thermal variation (° |)	11.7
Thermal conductivity of the soil (W m^{D}lF261^{1} K^{D}lF261^{1})	0.44
Density of the soil (kg	(mu | ^{D}lF261^{3})	1550
Specific heat of the soil (J kg^{D}lF261^{1} K^{D}lF261^{1})	1255
Thermal conductivity of the backfilling material (W m^{D}lF261^{1} K^{D}lF261^{1})	0.8
Depth of the backfilling material (m)	0.4
External radius of the backfilling material (m)	1.2

Reference

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Supplement No. 35

GUIDELINES CONCERNING THE MEASUREMENT OF WANDER

(Contribution from United States of America, referred to in

Recommendations G.812 and G.824)

Wander measurement methodology

The purpose of this Supplement is to present one suitable method of verification of timing accuracy of clocks. Guidelines concerning the measurement of jitter are contained in Supplement No. 38 of the O-Series.

1 Output wander measurement

1.1 *Slave clock*

The measurement strategy is to be able to derive the values of the model parameters contained in the Annex to Recommendation G.812 for the slave clock under test.

Once these parameter values have been obtained compliance with the specifications contained in Recommendation G.812 may be verified.

To adequately characterize the performance of a slave clock a series of tests must be performed. In general, the test fall into the three categories of operation:

1) ideal operation;

2) stressed operation;

3) holdover operation.

1.1.1 *Test configuration*

The objective of the test procedure is to be able to estimate the parameters in the clock model described above for a given clock under test. The architecture for a clock testing arrangement is shown in Figure 1. The components and their interconnection are described next.

Figure 1, (N), p.

1.1.1.1 *Reference clock*

The test configuration is designed to provide the clock under test with a primary rate digital reference timed from a stable reference oscillator. In clock testing, it is the relative phase-time compared to the reference input that is critical is important is that short-term instability of the reference oscillator be small to ensure low measurement noise and a low background tracking error in the control loop of the clock being tested.

In holdover testing, the longer term stability and drift of the reference oscillator is important.

1.1.1.2 *Digital reference simulation*

The testing arrangement is designed to provide a primary rate digital reference with impairment to the clock to allow for stress testing of the clock. To accomplish this a primary rate digital signal simulator and analyzer is employed that has the capability to be externally synchronized. For the 1544 kHz primary rate digital signal a 1544 kHz timing signal is supplied to the simulator/analyzer to control outgoing transmit timing. The 1544 kHz signal is produced via a distribution amplifier and synthesizer line tap. This distribution arrangement allows one to develop multiple taps of timing signals synthesized from the 10 MHz input from the reference oscillator. Each line tap is a dedicated synthesizer producing the timing signal required. The jitter produced from these synthesizers should be less than 1000 ps rms.

The primary rate impairment simulator is programmed via an IEEE 488 control bus to produce the desired interruption events to stress the clock. The primary rate digital signal is next bridged through a jitter generator and receiver. The jitter generator is used to insert background jitter to the digital signal. It is important to simulate a realistic level of background jitter for several reasons. Primarily, when interruptions occur the background jitter can be a major source of phase build-out error as the synchronization unit attempts to bridge the interruption. Secondly, the jitter transfer characteristics of the clock can be evaluated.

The jitter generation unit is provided an external jitter modulation input. The jitter signal used is bandlimited white noise. A signal from a white noise source is filtered using a low pass single pole filter with 150 Hz 3 dB cutoff. The main reason for lowpass filtering the jitter is to avoid producing bit errors from high frequency alignment jitter. The jitter power should be set to reflect realistic jitter levels in the network. It is important that sinusoidal jitter be avoided as a test jitter input, as certain phase detection techniques are very insensitive to sinusoidal jitter.

1.1.1.3 *Output timing signal recovery*

To test a clock, reference input is provided from the output of the jitter generator. To recover the output timing signal from the clock, an outgoing primary rate signal is selected from the unit controlled by the clock under test. This digital signal is connected to the receive portion of the Primary Rate Signal Simulator and Analyzer. In this unit the receiver timing function is decoupled from the transmit timing used in the generator. The receiver extracts a 4 kHz frame timing signal from the input signal and provides this timing signal at an external port. This 4 kHz timing signal is phase coherent with the outgoing timing from the clock under test.

1.1.1.4 *Phase-time data collection*

A counter is used to observe the relative phase-time error of the output 4 kHz timing signal compared to a reference 4 kHz timing signal. The reference 4 kHz timing signal is derived from the distribution amplifier and synthesizer units. The synthesizer jitter in generating the 4 kHz reference signal is less than 1000 ps. By performing the phase comparison at 4 kHz the observation range of phase variation is 250 µs. If care is given to start a test near the centre of this range, there should not be a problem associated with cycle slipping for all tests except holdover testing. However, even this range can be extended by resolving cycle slips in the data collection software.

In reality, the measurement resolution is limited by the intrinsic jitter in the counter as well as trigger error. Experience has shown that the measurement resolution jitter can be maintained below 100 ps rms with reasonable care given to cabling and trigger levels. More importantly, the overall background jitter noise level can be checked prior to testing to ensure proper performance. For the components used in the particular system described, overall jitter levels of 1000 ps rms are typically attainable. This is more than adequate for measuring the levels of phase stability expected from clocks.

The following discussion is applicable in an analogous manner to the 2048 kHz primary rate digital signal.

1.1.1.5 *Data collection*

An instrument control computer should be used to automate the testing procedure and collect and analyze the phase-time data. The control computer is interfaced via an IEEE 488 bus to both the Counter and the Primary Rate Digital Signal Simulator and Analyzer.

A key function of the control computer is to gather phase-time data from the counter. The instrument controller obtains a phase-time sample from the counter every 10 seconds. The counter is programmed to average 4000 samples over a 3 second window and return the average to the controller. The resulting measurement bandwidth is 0.33 Hz. The phase-time data is processed in real-time to obtain running estimates of the Allan variance for 10, 100, 1000 and 10 | 00 second observation intervals. The program also calculates a running estimate of the frequency departure and the drift.

1.1.1.6 *Data analysis*

The objective of the data analysis is to estimate from the data the parameters associated with the clock model. From the Allan variance data, one can determine the presence of either the white noise PM or white noise FM components expected from the model. The frequency departure estimator is the $y_{b\backslash di\backslash da\backslash ds}$term in the model, and the drift estimator D is the drift component in the model.

1.1.2 *Basic technique and procedure*

This paragraph contains the basic techniques and procedures for testing the three categories of slave clock operation. Appendix I provides examples of the application of these test using actual measurement data.

1.1.2.1 *Ideal operation*

The purpose of this testing is to obtain a baseline performance metric for a clock. The model predicts that clocks under ideal conditions should produce a white noise PM phase instability. This white noise PM should be small as it represents the best case performance of a clock (clearly less than 1 µs based on current MRTIE output requirements). It should be measured in the presence of realistic levels of jitter to assure acceptable jitter transfer.

In the standard test procedure described, the bandwidth of the measurement is 0.33 Hz. In some clock designs, there is significant noise between this 0.33 Hz cutoff and the 10 Hz cutoff associated with jitter. It is important to evaluate the jitter in this band. This could be accomplished by developing an additional measurement program to capture this fast wander data.

1.1.2.2 *Stressed operation*

This area of testing is critically important to adequately evaluate clocks. The difficulty in this testing is selection of the appropriate disruption events. For some clocks any event that appears as a severely errored second will produce a phase build-out event. In some clocks any outage or spurious noise spikes will perturb a counter in the phase detection producing a spurious phase hit which may or may not be phase built-out depending on its severity. On the other hand, clocks can be designed to observe the framing pulse position to extract phase. In such clocks, an interruption need not produce a phase build-out event unless there is an actual shift in the framing pulse position (for example a protection switch event).

It is proposed that one stress test which should be performed is to simulate an SES event with a short outage (100 ms) at a rate of 10 SES per day in the presence of background input jitter. Typically an outage of this magnitude will force a clock to attempt to phase build-out without switching references. An example of this stress test is given in the next section and should serve to clarify the concepts and the significance of the results.

Other stress inputs should also be considered in evaluating a clock.

— *Error bursts* | An error burst can be simulated in which the underlying timing waveform is not perturbed. Under this condition, it would be advantageous for a clock not to phase build-out. Such a test would gain in importance if it is determined that the majority of error burst events are actually pure data errors with no perturbation in timing.

— *Phase bit* | Phase hits are produced by protection activity, as well as from other clocks. Phase hits are interruption events that should either force a phase build-out event or inadvertently be followed by the clock. In either case they will degrade a clock's performance. This is an area for further study.

— *Restart events* | Restart events are a phenomena associated with certain clocks. A restart event is associated with a clock giving up its current state, and defaulting back to its initial conditions. The results are a transient event which can be significant. Restart events should not happen during normal clock operation, and thus should not likely be included in a general clock testing plan. However, it is important that the behaviour be better understood and controlled.

— *Frequently hit* | It is important that clocks do not follow references that exhibit large frequency hits. However the ability to detect frequency hits is closely tied to the selection of the tracking bandwidth of a given clock PLL. The solution to the problem will depend on the degree to which the bandwidth of various clocks in a network can be standardized.

1.1.2.3 *Holdover operation*

In holdover testing, the objective is to estimate the initial frequency offset ($y_{b\backslash di\backslash da\backslash ds}$) and the Drift (D) of the clock model. The initial frequency offset is dependent on the accuracy of the frequency estimate obtained in the control loop, and the frequency settability of the local oscillator. It is important to test holdover from a reasonable stress condition prior to holdover to capture the control loops capability of obtaining an accurate frequency estimate.

In determining the drift estimate, one critical factor for quartz oscillators is that it typically takes observation intervals lasting over days to obtain a statistically significant drift estimator. This is a hard reality that cannot be avoided. In addition, attention must be placed on the temperature conditions maintained during the test. This is a subject for further study.

1.2 *Primary reference clock*

This section requires further study.

APPENDIX I
(to Supplement No. 35)

Example applications

This section presents the results of the application of some of the testing procedures for two clocks. It is important to point out that the two clocks tested have different internal architectures. The main result of the tests is that the model for clock performance was supported. This model can be summarized as follows:

1) For short observation intervals outside the tracking bandwidth of the PLL, the stability of the output timing signal is determined by the short-term stability of the local synchronizer time base.

2) In the absence of reference disruptions, the stability of the output timing signal behaves as a white noise PM process as the observation period is increased to be within the tracking bandwidth of the PLL.

3) In the presence of disruptions, the stability of the output timing signal behaves as a white noise FM process as the observation period is increased to be within the tracking bandwidth of the PLL.

4) In the presence of disruptions, the output timing signal may incur a systematic frequency offset with respect to the reference. This results from a bias in the phase build-out when reference is restored.

The specific test results are described below.

I.1 *Local clock evaluation*

The results described in this section are for actual performance data.

I.1.1 *Unstressed primary rate input tests*

The first test performed was to evaluate the timing signal output under ideal reference input conditions. The primary rate reference input is produced by the generator timed from the Caesium reference. The jitter outside the tracking bandwidth of the stratum 3 PLL is much less than 1 ns. Typically, 300 ps as measured by the counter.

For this test, the jitter test set was bypassed, and the primary rate from the primary rate simulator and analyzer was fed directly into the synchronizer. The test was run for 67 hours. The results are presented in Figure I-1. The square root of the Allan variance is plotted vs. observation time. The data points marked by triangles apply to this test.

The test results are consistent with the model. For observation times outside the tracking bandwidth of this PLL (less than 60 seconds), the Allan variance indicated a white FM noise resulting from the local quartz oscillator. As the observation time increases, the PLL tracks the reference and the noise process converges to white FM.

The magnitude of the white PM noise is 85 ns rms. One component of this noise is the rms time error of the oscillator in 60 seconds (the bandwidth of this PLL is 1/60 sec). In addition, there is a component resulting from the resolution of the phase detector. A phenomena that arises in digital loops is that the phase error can make excursions of at least one bit in either direction of the nominal setpoint. This effect is reduced when the input has jitter on the order of a phase detector bit.

I.1.2 *Stressed primary rate input test*

The purpose of this test is to emulate the behaviour of the synchronizer under stress conditions that arise in actual networks. For this test, a short outage event was produced under program control by the primary rate simulator and analyzer every 15 minutes. The outage events duration was randomized with a uniform distribution over the range of 10 to 100 ms.

For this test, the jitter set was bypassed, and the primary rate signal from the primary rate simulator and analyzer was fed directly into the synchronizer. The test was run for 50 hours. The results are presented in Figure I-1. The square root of the Allan variance is plotted vs. observation time. The data points marked by plus signs apply to this test.

I.1.2.1 *Allan variance results*

The test results are consistent with the model. For observation times outside the tracking bandwidth of this PLL (less than 60 seconds), the Allan variance indicates a white FM noise resulting from the local quartz oscillator. As the observation time increases, the PLL is experiencing a disruption every 900 seconds. The residual phase build-out error accumulates and produces a random walk in phase (white noise FM). The build-out error per disruption is calculated as 180 ns rms.

I.1.2.2 *Systematic frequency offset*

The stress test data shows a statistically significant frequency offset. The frequency offset over the 50 hour test was 3×10^{-11}. Given the white FM noise, the rms error is 1.5×10^{-11}. These numbers reflect a bias error in the phase build-out in the range of 15 to 45 ns. Such bias errors in clocks result in frequency offsets. The implications of this is that to some extent all clocks in a network operate plesiochronously. Given a worse case level of disruption of ten per day the resulting frequency offset is of the order of parts in 10^{12}.

Figure I-1, (N), p.17

I.1.2.3 *Significance of stress test results*

To obtain a meaningful interpretation of the stress test results one must consider the disruption level. In this test the disruption level was 100 disruptions per day. This is an order of magnitude greater than what can be expected on actual primary rate links. In this particular PLL the build-out error process is independent from one event to the next. This can be proven by testing at several disruption levels. The results indicated a rms error of 180 ns per disruptions. Given 10 disruptions per day the resulting daily rms error is 570 ns.

I.2 *Transit clock evaluation*

The results described in this section are for actual performance data.

I.2.1 *Unstressed primary rate input test*

The first test performed was to evaluate the timing signal output under ideal reference input conditions. The primary rate reference input is produced by the primary rate simulator and analyzer timed from the Caesium reference. The jitter outside the tracking bandwidth of the stratum 3 PLL is much less than 1 ns. Typically, 300 ps as measured by the counter.

For this test, the jitter test set was included. The jitter test set was given an external jitter modulation input. The jitter signal was band limited white noise. A single pole filter was employed with a 150 Hz 3 dB cutoff. The jitter was low passed filter to avoid producing framing errors resulting from high frequency alignment jitter. The external signal was adjusted to achieve a peak-to-peak jitter level of 1.5 µs. The test was run for 23 hours. The results are presented in Figure I-2. The square root of the Allan variance is plotted vs. observation time. The data points marked by triangles apply to this test.

The test results are consistent with the model. For observation times outside the tracking bandwidth of this PLL (less than 450 seconds), the Allan variance indicated a white FM noise resulting from the local quartz oscillator. As the observation time increases, the PLL tracks the reference and the noise process converges to white PM.

The magnitude of the white PM noise is 6 ns rms. This is an exceptionally good number and results from the tight time constant for the loop (450 seconds). In this case the input jitter prevents the edge jumping effects.

Figure I-2, (N), p.

I.2.2 *Stressed primary rate input test*

The purpose of this test is to emulate the behaviour of the synchronizer under stress conditions that arise in actual networks. For this test, a short outage event was produced under program control by the primary rate simulator and analyzer every 30 minutes. The outage events duration was randomized with a uniform distribution over the range of 10 to 100 ms.

For this test, the jitter test set was included. The jitter test set was given an external jitter modulation input. The jitter signal was bandlimited white noise. A single pole filter was employed with a 150 Hz 3 dB cutoff. The jitter was low passed filter to avoid producing framing errors resulting from high frequency alignment jitter. The external signal was adjusted to achieve a peak-to-peak jitter level of 1.5 µs. The test was run for 70 hours. The results are presented in Figure I-2. The square root of the Allan variance is plotted vs. observation time. The data points marked by plus signs apply to this test.

I.2.2.1 *Allan variance results*

The test results are consistent with the model. For observation times outside the tracking bandwidth of this PLL (less than 450 seconds), the Allan variance indicated a white FM noise resulting from the local quartz oscillator. As the observation time increases, the PLL is experiencing a disruption every 1800 seconds. The residual phase build-out error accumulates and produces a random walk in phase (white noise FM). The build-out error per disruption is calculated at 34 ns rms. A contributor to this error is the input primary rate jitter. The algorithm averages the input to improve the estimate of the phase error to build-out.

I.2.2.2 *Systematic frequency offset*

The stress test data shows a statistically insignificant frequency offset. The frequency offset over the 70 hour test was 6×10^{D}lF261^{13}. Given the white FM noise, the rms error is 1.5×10^{D}lF261^{12}. Given this uncertainty, there is no indication of a bias in the data. In the worse case the bias should not be more than the uncertainty level of 1.5×10^{D}lF261^{12}.

I.2.2.3 *Significance of stress test results*

To obtain a meaningful interpretation of the stress test results one must consider the disruption level. In this test the disruption level was 48 disruptions per day. This is five times greater than what can be expected on actual primary rate links. In this particular PLL the build-out error process should be independent from one event to the next based on a knowledge of the PLL design. This can be proven by testing at several disruption levels. The results indicated an rms error of 34 ns per disruption. Given 10 disruptions per day, the resulting daily rms error is 100 ns.

I.3 *Allan variance confidence limits*

Sample variances (like sample Allan variances) are distributed as chi-square. Based on J. Barnes work described in [1], the confidence interval for the Allan variance can be determined assuming a given noise process. In calculating the sample Allan variances a complete overlap of lag intervals was used. This is the most efficient use of data. However, it is incorrect to assume independence in overlapping samples when calculating confidence intervals. This is described in complete detail in [1]. For brevity, the methods for calculating the confidence interval described in reference [1] were employed.

The 90% confidence factors for white PM noise are bounded within 0.9 and 1.1 for all lag times up to 10,000 assuming an observation period of a day. For white FM noise over a day observation interval the confidence factors were as follows. For 1000 second lag interval the lower bound is 0.9, and the upper bound is 1.2. At 10 | 00 the confidence factors are 0.75 and 1.5.

As an example of what these factors mean consider the white FM noise component in Figure I-2 (plus sign tagged data). For the 10 | 00 second lag, the square root of the sample variance is 8×10^{D}lF261^{12}. The 90% confidence interval for the true variance is bounded by the confidence factors multiplied by the sample variance. This leads to the square root of the Allan variance being bounded between 6.9×10^{D}lF261^{12} and 9.8×10^{D}lF261^{12} with a 90% confidence level.

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Supplement No. 36

JITTER AND WANDER ACCUMULATION IN DIGITAL NETWORKS

(Referred to in Recommendation G.824)

The present Supplement describes a model which has been used to compute jitter/wander accumulation in digital networks arising from cascaded digital regenerators and asynchronous digital multiplexes. This model does not include other sources of wander generation; e.g., environmental, disruptions in synchronization reference distribution, etc.

1 Jitter and wander accumulation — Digital regenerator component

The most widely used model of regenerator jitter/wander accumulation, attributed to Chapman [1], treats the regenerator as linear, shift-invariant system. In order to compute the accumulated jitter/wander after N cascaded regenerators, intrinsic regenerator jitter/wander is categorized in terms of ‘‘random’’ and ‘‘systematic’’ components. Chamzas model of regenerator jitter/wander accumulation [2] addresses how stochastic variations in regenerator retiming circuits affect jitter/wander accumulation. The results of this study demonstrate that use of the appropriate *mean* jitter/wander transfer characteristic in the identical regenerator accumulation model, summarized above, provides a very good estimate to jitter/wander accumulation computed assuming a stochastic variation of retiming circuits.

Using Chapman's model for a chain of N *identical* | regenerators, defining $H_1(j\ \omega)$ as the jitter/wander transfer characteristic for one regenerator, and redefining the random and systematic components as completely uncorrelated and correlated components, respectively,

— the power spectral density of the random jitter/wander component is:

where ?71 $$Ei:*R* :*i* 1_ | is the constant, internally generated, random (pattern independent plus uncorrelated pattern dependent) jitter/wander power spectral density for one regenerator.

— the power spectral density of the systematic jitter/wander component is:

where ?71 $$Ei:*S* :*i* 1_ | s the constant, internally generated, systematic (correlated pattern dependent) jitter/wander power spectral density for one regenerator. ?71 $$Ei:*R* :*i* 1_ and ?71 $$Ei:*S* :*i* 1_ can be estimated from practical measurements based upon the regenerator's jitter/wander response to short and long word lengths from a pattern generator, and correlation studies.

When there is no peaking in the regenerator jitter/wander transfer characteristic, the systematic jitter/wander accumulates much more rapidly than the random jitter/wander [1], [4], [5]; as a result, random jitter/wander accumulation is often ignored. However, for a large number of regenerators with peaking in the jitter/wander transfer characteristic, the total jitter/wander accumulation can be dominated by the random component.

2 Jitter and wander accumulation — Asynchronous digital multiplex component

With Gaussian input jitter/wander, having an rms amplitude of σ, and double-sided power spectral density $\theta_{in}(f)$, the unfiltered multiplex intrinsic jitter/wander is given by [6].

p Multiplexer stuffing ratio

f jitter/wander frequency normalized by the multiplexer maximum suffising frequency

3 Method of combination

Assuming that the jitter/wander accumulation from each component part can be modeled by filtered Gaussian randam variables, the power spectrum and rms amplitude after each component part is computed as the accumulation due to the preceding parts according to the following rules [3]:

i) The jitter/wander spectrum at the output of a chain of regenerators is the power sum of the jitter/wander generated by the regenerators (equations [1] and [2]) and any jitter/wander at the input of the chain, appropriately filtered by the equivalent jitter/wander transfer characteristic. Thus, for input jitter/wander, $\theta_{in}(\omega)$, the output jitter/wander, $\theta_{out}(\omega)$, is given by

ii) The jitter/wander spectrum at the output of a demultiplexer is the power sum of the unfiltered intrinsic multiplex jitter/wander and the accumulated higher rate input jitter/wander, attenuated by the desynchronizer jitter/wander transfer characteristic. Thus, if $\theta_{in,1}(\omega)$ is the unfiltered intrinsic multiplex jitter/wander and $\theta_{in,2}(\omega)$ is the accumulated higher rate input jitter/wander, the output jitter/wander, $\theta_{out}(\omega)$ is given by

where r | is the ratio of the multiplexer output frequency to tributary frequency, and $G(j\omega)$ represents the desynchronizer jitter/wander transfer characteristic.

The following equations are valid for both single- and double-sided power spectra and corresponding transfer characteristics.

4 Definition of peak-to-peak jitter/wander amplitude

The probability that the jitter/wander exceeds a particular threshold amplitude | | fIx | n times in the time interval (t , t + ?63t) may be described by a Poisson density function [3].

where N | x) is the average number of times/second that the threshold | | fIx | is exceeded.

For Gaussian jitter/wander, with double-sided power spectral density θ(ω), N | x) is given by [7]

The probability that the jitter/wander doesn't exceed the threshold during the time interval (t , t + ?63t) is

Solving for the threshold,

If we assume that each time the threshold is crossed, an undesirable event (impairment) may result, the mean time between impairments, MTBI, may be taken as

Thus, equation (9) may be expressed as

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