5i’

FASCICLE III.5

Recommendations G.801 to G.961

DIGITAL NETWORKS, DIGITAL SECTIONS

AND DIGITAL LINE SYSTEMS

Blanc

MONTAGE: PAGE 2 = PAGE BLANCHE

SECTION 8

DIGITAL NETWORKS

8.0 General aspects of digital networks

Recommendation G.801

DIGITAL TRANSMISSION MODELS

(Malaga-Torremolinos, 1984)

The CCITT

considering

(a) that digital networks support a wide variety of connections for which digital transmission impairments and other performance parameters need to be controlled;

(b) that, if proper control is not exercised, then under certain circumstances, digital transmission impairments cause unacceptable service degradations;

(c) that various network performance objectives need to be allocated to the elements of a digital network;

(d) that equipment design objectives need to be formulated for individual digital elements;

(e) that networks need to be configured to a level of transmission quality consistent with the needs of different services (voice and non-voice) and in particular of services in the ISDN;

(f) that Administrations need to examine the effect on transmission quality of possible changes of impairment allocation in national networks;

(g) that there is a need to test national rules for prima facie compliance with any impairment criteria which may be recommended by the CCITT for national and international systems;

(h) that guidelines need to be formulated governing the use of certain digital elements (e.g. satellite links, transcoders, digital pads, circuit multiplication devices, etc.),

recommends

that in the study of digital transmission impairments and other performance parameters, the following network models and associated guidelines should be applied.

1 Introduction

Digital transmission network models are hypothetical entities of a defined length and composition for use in the study of digital transmission impairments (e.g. bit errors, jitter and wander, transmission delay, availability, slip, etc.). The diversity of possible network situations requires that individual models can only represent a small portion of typical real entities. However, a limited number of such models (e.g. 2 or 3) together may be sufficiently representative to provide a useful tool upon which studies may be based.

The network models, where applicable, take account of the following features:

a) physically reflect the length of the overall connection with some indication of frequency of occurrence,

b) identify boundaries between switching and transmission elements,

c) give no indication of the means of implementing transmission between switching elements (e.g. metallic, optical, radio media, satellite etc.),

d) describe in detail the user/network access arrangement in the local portion (i.e. customer to local exchange),

e) take account of all possible usages or be independent of them,

f) reflect the use of additional digital processing elements required in particular network configurations (e.g. A-μ converters, digital pads, transcoders, etc.).

This Recommendation makes no statement in respect of the electrical and physical environment in which the network models operate. These aspects are currently the subject of study. In the application of these network models to the study of specific digital impairment (e.g. errors) arbitrary judgements may need to be made concerning the significance, in particular, of the electrical environment.

2 Hypothetical reference connection (HRX)

A digital HRX is a model in which studies relating to overall performance may be conducted, thereby facilitating the formulation of standards and objectives. In order to initiate studies directed at the performance of an ISDN, an all digital 64 kbit/s connection is considered. Since the overall network performance objectives for any performance parameter need to be consistent with user requirements, such objectives, in the main, should relate to a network model which is representative of the very long connection. The HRX shown in Figure 1/G.801 serves this purpose. It does not represent the rare worst case connection; although it does aim to encompass the vast majority of connections for each relation. Moreover, the difficulty of identifying every conceivable practical implementation of a connection and the undesirability of producing too many options naturally requires that this ‘‘standard HRX’’ may need to be appropriately modified in composition to suit the particular task in

hand. A situation can be envisaged where many similar HRXs exist to serve specific functions, but in all cases they are derivatives of the ‘‘standard HRX’’. The potential proliferation of HRXs prevent their inclusion in this Recommendation. Any departure from the ‘‘standard HRX’’ may need to be shown in the Recommendation appropriate to that impairment or performance parameter. For example, see Recommendation G.821. They are not intended to be used for the design of transmission systems.

The diversity in composition is particularly apparent when a distinction is made between average size and large countries and, therefore no one HRX can possibly accommodate such variations. In the process of apportionment the demarcation between national and international portions is unimportant as in most instances the intrinsic quality of circuit comprising both portions is the same. In contrast, however, the overall length is regarded as being critical and its choice is ‘‘country size’’ independent. Accordingly, the level of impairment actually experienced over a real connection is considered satisfactory if compatible with that stipulated for the longest HRX, taking due account of differences between the construction of the hypothetical and real connections. For a large proportion of real connections configured using equipment designs recommended by CCITT, the actual performance is likely to be significantly better. Those CCITT compliant connections which exceed the longest HRX in either length or complexity may not have controlled levels of performance; however, their impairment levels are unlikely to exceed those of the longest HRX by more than a factor of 2 and the design margins provided with individual items of equipment may well bring the impairment to within CCITT end-to-end performance specifications.

In formulating the above HRX no account was taken of the following aspects:

— maritime applications,

— semi-automatic connections (i.e. auto-manual),

— standby routing in case of failure.

Two other HRXs have been included to facilitate studies over shorter connections with a view to establishing the typical performance levels likely to be achieved over frequently realized international circuits. These are given in Figures 2/G.801 and 3/G.801.

Figure 1/G.801, p. (a l’italienne)

Figure 2/G.801, p.

FIGURE 3/G.801, p.

3 Hypothetical reference digital link (HRDL)

To facilitate the study of digital transmission impairments (e.g. bit errors, jitter and wander, slip, transmission delay) it is necessary to define network models comprising a combination of different types of transmission elements (e.g. transmission systems, multiplexers, demultiplexers, digital pads, transcoders). Such a model is defined as a Hypothetical Reference Digital Link (HRDL). The exact length and composition in respect of the number, type and disposition of equipments will depend on the digital impairment under study. For example, in the analysis of jitter accumulation in a network both transmission systems and muldexes would need to be included to take account of the different jitter characteristics exhibited by such equipment types. In addition the HRDL can be regarded as a constituent element of an HRX thus permitting the apportionment of overall performance objectives to a shorter model. A length of 2500 km is considered as a suitable distance for a HRDL.

The formulation of such models is the subject of further study.

In CCIR Recommendations the term Hypothetical Reference Digital Path (HRDP) is sometimes used. This is equivalent to a Hypothetical Reference Digital Link (see Definition 3005 in Recommendation G.701).

4 Hypothetical reference digital section (HRDS)

To accommodate the performance specification of transmission systems (i.e. digital line and radio systems) it is necessary to introduce a Hypothetical Reference Digital Section (HRDS). Such a model is defined in Figure 4/G.801 for each level in the digital hierarchies defined in Recommendation G.702. The input and output ports are the recommended interfaces as given in Recommendation G.703 for hierarchical bit rates. The lengths have been chosen to be representative of digital sections likely to be encountered in real operational networks, and are sufficiently long to permit a realistic performance specification for digital radio systems. The model is homogeneous in that it does not include other digital equipments such as multiplexers/demultiplexers. This entity can form a constituent element of a HRDL.

Figure 4/G.801, p.

It is possible to relate the two following types of performance requirement to an HRDS:

— the Network Performance Objectives (NPO) which are the objectives to be realized in a real network;

— the Equipment Design Objectives (EDO) which provide guidance to the designer of systems using specific transmission media and transmission techniques.

Note 1 — The Equipment Design Objectives which normally appear in the appropriate transmission and switching system recommendations are formulated to ensure compatibility with the corresponding network performance objectives.

Note 2 — An explanation of a Network Performance Objective and an Equipment Design Objective is given in Recommendation G.102.

Note 3 — The formulation of a homogeneous entity of a realistic length permits specification and commissioning acceptance testing under real operational conditions.

In a similar manner CCIR and CMTT have formulated media and application orientated models for use in their studies. The following recommendations describe the relevant models.

— Recommendation 502-2 (Draft). Hypothetical Reference Circuit for Sound Programme Transmission. (Terrestrial systems and systems in the fixed-satellite service).

— Recommendation 521-1. Hypothetical Reference Digital Path for systems using digital transmission in the fixed-satellite service.

— Recommendation 556. Hypothetical Reference Digital Path for radio-relay systems for telephony.

ANNEX A

(to Recommendation G.801)

The application of
Hypothetical Reference Models

in the formulation of equipment design objectives

An important use of hypothetical reference models is to facilitate the apportionment of network performance objectives to constituent elements, prior to the derivation of equipment design objectives. To satisfactorily achieve this objective a diagrammatic representation of the approach adopted by CCITT in the formulation of equipment design objectives is shown in Figure A-1/G.801.

The approach recognizes that it may be necessary to derive from the ‘‘standard HRX’’ a more appropriate HRX which better takes into account both the usage and the specific network performance parameter under study. The adoption of this approach will facilitate the formulation of rules governing the use of certain digital elements such as satellite links, transcoders, digital pads, etc.

National Administrations are advised to develop their own representative network models reflecting the features of their evolving national digital network in order to validate prima facie compliance with international standards.

FIGURE A-1/G.801, p.5

Recommendation G.802

INTERWORKING BETWEEN NETWORKS

BASED ON DIFFERENT DIGITAL HIERARCHIES AND SPEECH ENCODING LAWS

(former Recommendations G.722 of Volume III of

the Yelow Book, further amended)

1 Introduction

This Recommendation deals with the following aspects of interworking between networks for transport of 64 kbit/s digital information:

— encoding law and conversion rule for interworking between networks using the different encoding laws based on Recommendations G.711, G.721 and G.722;

— interworking hierarchy between networks which incorporate the different digital hierarchies based on Recommendation G.702;

— interworking arrangements between networks incorporating the different hierarchies and encoding laws; and,

— interconnection by plesiochronous operation between networks which each has an independent synchronization.

This Recommendation is applicable also to ISDNs for transport of B channels specified in Recommendation I.412.

Note — The future specifications on channels and their bit rates to support ISDN broadband services for customer-to-customer applications may require additional interworking arrangement specifications other than those specified below.

2 Terms and definitions

The terms used in this Recommendation and not defined below are described in Recommendations G.701 or I.112.

2.1 z-operation

Conversion of the µ-law character signal ‘‘00000000’’ (all-zero octet) into the µ-law character signal ‘‘00000010’’, where ‘‘1’’ is the bit numbered seven in the octet (see Recommendation G.711).

Note — Bit number indicates the chronological order of transmission of bits in serial processing.

2.2 1.5/2 Mbit/s multiplex system conversion (1.5/2 Mbit/s MSC)

A function which embodies the following properties:

1) termination of a digital link operating at a digital hierarchical level of 1544 kbit/s;

2) termination of a digital link operating at a digital hierarchical level of 2048 kbit/s; and,

3) rearrangement of 64 kbit/s channels between 1544 kbit/s and 2048 kbit/s digital terminations.

Note — The hierarchical levels and the frame structures are specified in Recommendations G.702 and G.704, respectively.

2.3 pulse density requirement (PDR) at 1544 kbit/s

The minimum requirement for an entire 1544 kbit/s digital signal is that there should be no more than 15 binary ‘‘0’’s between successive binary ‘‘1’’s and that there should be an average binary ‘‘1’’s density of at least one in every eight bits. This requirement is due to the design of a number of existing systems (see Recommendation G.703.)

Moreover, the requirement for an octet-structured source in a 1544 kbit/s digital link is that at least one binary ‘‘1’’ should be contained in any octet.

3 Unrestricted 64 kbit/s transfer capability of a digital link

Newly introduced digital transmission systems should have the capability to provide bit sequence independence for 64 kbit/s digital links. This capability should be activated as soon as unrestricted 64 kbit/s transfer capability can be practically realized.

During a transition period, however, 56 kbit/s bit sequence independent transfer capability may be provided by bilateral agreement. (Important constraints on the data formats transmitted by source data terminal equipment are given in Annex 1 to this Recommendation.)

4 Encoding law conversion between A-law and μ-law

4.1 *Encoding law on an international digital link*

International digital links between countries which have adopted different PCM encoding laws (A-law or μ-law) should carry signals encoded in accordance with the A-law specified in Recommendation G.711.

Where both countries have adopted the same law, that law should be used on digital links between them.

4.2 *Conversion rule*

A-law/μ-law conversion necessary between countries which have adopted different PCM encoding laws will be performed according to Recommendation G.711 by the μ-law country. The conversion includes the even-bit inversion of the A-law character signal.

Note — Location of the conversion function in a μ-law country is a national matter depending upon the structure of domestic digital networks, and is left to the discretion of the Administrations in the μ-law country.

4.3 *Control of conversion function*

In switched public network applications enabling/disabling of the conversion function should be under control of the international switching system, and will be carried out on a call-by-call or during-a-call basis depending upon the service category requested by the signalling protocol.

It should also be possible to enable/disable this conversion function manually and/or via an operator terminal on a per-channel or semi-permanent basis. This capability would be necessary for configuring leased line circuits not passing through the international switching system, or if the international switching system were not capable of controlling this function.

Note — Control of conversion function in ISDN environment is specified in I.300-series and I.500-series Recommendations.

5 Interworking hierarchy

For international interworking between networks using different digital hierarchies specified in Recommendation G.702, the following interworking hierarchy should be employed:

2048 | (em | 312 | (em | 4 | 36 | (em | 39 | 64 kbit/s.

For interworking between networks with different digital hierarchies but with 1544 kbit/s primary level, however, levels other than those specified for the above interworking hierarchy may be employed (e.g. 1544 kbit/s).

Note 1 — National networks with a 1544 kbit/s primary level may offer transit of international traffic of 6312 kbit/s composed of three 2048 kbit/s signals or of 44 | 36 kbit/s containing twenty-one 2048 kbit/s signals. These networks will provide the property of bit sequence independence at 6312 and 44 | 36 kbit/s and hence at 2048 kbit/s.

Note 2 — The frame structures for 2048-6312 kbit/s, 6312-44 | 36 kbit/s and 44 | 36-139 | 64 kbit/s multiplexing stages are specified in Recommendations G.747, G.752 and G.755, respectively.

6 Interworking arrangements

Based on the general specifications described in the previous Sections, establishment of an international digital interconnection between networks using the different digital hierarchies and speech encoding laws should conform to the interworking arrangements specified in Table 1/G.802.

7 Transport of a 1544 kbit/s signal within a G.704-structured 2048 kbit/s signal

For international leased line applications, the transmission of 1544 kbit/s signals may be considered using a special mapping into point-to-point 2048 kbit/s signals. Annex B to this Recommendation specifies the method for this mapping.

Note — The possible development of specific mappings of 8448 or 34 | 68 kbit/s signals into 44 | 36 kbit/s signals is not precluded.

8 Synchronization of an international digital link

8.1 *Links not synchronized to the national networks*

Where independently synchronized national networks are interconnected via an international digital link, the timing of which is independent of the national networks, the link should be operated in a plesiochronous mode with the accuracy specified in Recommendation G.811.

8.2 *Links synchronized to the network in the transmitting country*

Where independently synchronized national networks are interconnected via an international digital link, the timing of which is synchronized to the national network in the transmitting country, the plesiochronous operation will be performed in the receiving country.

H.T. [T1.802]

TABLE 1/G.802

Interworking arrangements

Type of information Signalling information (Note 1) }	Voice or voiceband data		Non-voice information		{					
{ Encoding law at IRP (Note 2) Function }	PCM G.711		ADPCM G.721		SB-ADPCM G.722		------		------	
Network (Note 3)	A	B	A	B	A	B	A	B	A	B
1.5/2 Mbit/s MSC	—	X	—	X	—	X	—	X	—	X
A/μ and μ/A conversion	—	X	—	—	—	—	—	—	—	—
Z-operation	—	X (Note 4)	—	X (Notes 4 and 5)	—	X (Notes 4 and 6)	—	X (Note 4)	—	—
Transcoding	—	—	X	X	—	—	—	—	—	—

Note 1 — Signalling information is transferred on unrestricted channels between International Switching Centers (ISCs).

Note 2 — IRP = Interworking reference point between Network A and Network B.

Note 3 — ‘‘A’’ is a network within the country incorporating the A-law and 2048 kbit/s-based digital hierarchy. ‘‘B’’ is a network within the country incorporating the μ-law and 1544 kbit/s-based digital hierarchy.

Note 4 — Z-operation in the μ-law country will be applied when the link in that country contains transmission systems that have to meet PDR; in this case unrestricted 64 kbit/s transfer capability cannot be provided due to PDR and the bit sequence independent transfer capability is restricted to 56 kbit/s.

Note 5 — 32 kbit/s digital signals, which are voice or voiceband data signals encoded in accordance with the ADPCM algorithm specified in Recommendation G.721, do not contain a ‘‘0000’’ code word. (See Recommendation G.721.) This implies that even when PDR exists in the μ-law country, these signals will not be affected by the z-operation and will be transferred transparently.

Note 6 — 64 kbit/s audio signals, where the audio signals having the bandwidth of 50 to 7000 Hz are encoded at 64, 56 or 48 kbit/s in accordance with the coding algorithm specified in Recommendation G.722, do not contain an all-zero octet. (See Recommendation G.722.) This implies that even when PDR exists in the μ-law country, these signals will not be affected by the z-operation and will be transferred transparently.

Tableau 1/G.802 [T1.802], p.

ANNEX A

(to Recommendation G.802)

Impact on terminal equipment designed to work with 56 kbit/s bit sequence independent transfer capability

During a transition period 56 kbit/s bit sequence independent transfer capability may be provided by bilateral agreement. In this case a 56 kbit/s bit sequence independent transfer capability requires that the source data terminal equipment (DTE) fix the eighth bit of each octet to binary ‘‘1’’. This must be done on both ends of the digital connection even if one portion of the connection has unrestricted 64 kbit/s transfer capability. Failure to keep the eighth bit fixed to binary ‘‘1’’ will cause any all-zero octet to be converted to ‘‘00000010’’ by z-operation in the μ-law country.

ANNEX B

(to Recommendation G.802)

Mapping method of a 1544 kbit/s signal into a G.704-structured 2048 kbit/s signal

The following is a means of accommodating a bit synchronous 1544 kbit/s signal, which may be unstructured or structured, within a G.704-structured 2048 kbit/s frame, for the purpose of providing leased line applications at 1544 kbit/s only. The 1544 kbit/s signal is transmitted transparently without regard to its frame structure within the 2048 kbit/s signal.

The 193 bits of an arbitrary 125 μs period of the 1544 kbit/s signal should be accommodated within a G.704-structured 2048 kbit/s frame as follows:

TS 0: Frame alignment signal according to Recommendation G.704

TS 1-15

TS 17-25 193 contiguous bits of the 1544 kbit/s signal

Bit 1 in TS 26

TS 16, 27-31: Reserved for possible accommodation of additional information at up to 384 kbit/s (Note 2)

Note 1 — In cases where only the 1544 kbit/s signal is to be transported, the timing of the 1544 kbit/s (or 2048 kbit/s) outgoing signal should be derived from the 2048 kbit/s (or 1544 kbit/s) incoming signal for each direction of transmission.

Note 2 — In some cases, e.g. where information is transported by the reserved time-slots, the timing of the outgoing signal should be traceable to the national reference clock conforming to Recommendation G.811. This will require the use of 125 μs slip buffers.

Note 3 — The maximum capacity available to end-users for transparent transport of their information is 1536 kbit/s and not 1544 kbit/s. Depending on the national regulations some network operators may offer the user of part of the 8 kbit/s overhead associated with a 1544 kbit/s signal for performance monitoring and its reporting.

8.1 Design objectives for digital networks

Recommendation G.810

CONSIDERATIONS ON TIMING AND SYNCHRONIZATION ISSUES

(Melbourne, 1988)

1 General

This Recommendation provides information and guidance concerning the various timing and synchronization Recommendations as well as insight into the fundamental related issues.

2 Definitions

primary reference clock

A reference clock that provides a timing signal with long term frequency departure maintained at 1 | (mu | 0^{D}lF261^{11} or better with verification to Universal Time Coordinated (UTC). Requirements for primary reference clocks are given in Recommendation G.811.

Note 1 — The primary reference clock may generate a timing signal completely autonomous of other references or alternatively, the primary reference clock may not have a completely autonomous implementation, in which case it may employ direct control from standard UTC-derived frequency and time sources.

Note 2 — This clock is sometimes referred to as a Stratum 1 clock (i.e. the highest quality clock in the network).

synchronous network node

A geographical location at which there are one or more interconnected synchronous digital equipments.

transit node

A synchronous network node which interfaces with other nodes and does not directly interface with customer equipment.

local node

A synchronous network node which interfaces directly with customer equipment.

slave clock

A clock whose timing output is phase-locked to the timing signal received from a higher quality clock. Requirements for slave clocks are given in Recommendation G.812.

Note — The highest quality slave clock is sometimes referrred to as a transit node clock, or a Stratum 2 clock. The second highest quality slave clock is sometimes referred to as a local node clock, or a Stratum 3 clock.

jitter

Short-term variations of the significant instants of a digital signal from their reference positions in time.

timing jitter

The short term variations of the significant instants of a digital signal from their ideal positions in time (where short term implies these variations are of frequency greater than or equal to 10 Hz).

alignment jitter

The short term variations between the optimum sampling instants of a digital signal and a sampling clock derived from it.

wander

The long term variations of the significant instances of a digital signal from their ideal positions in time (where long term implies that these variations are of frequency less than 10 Hz).

Note — For the purposes of this Recommendation and the following related Recommendations, this definition of wander does not include integrated frequency departure.

frequency departure

An underlying offset in the long term frequency of a timing signal from its ideal frequency.

slip

The repetition or deletion of a block of bits in a synchronous or plesiochronous bit stream due to a discrepancy in the read and write rates at a buffer.

3 Description of phase variation components

Phase variation is commonly separated into three components: jitter, wander and integrated frequency departure. In addition, phase discontinuities due to transient disturbances such as network re-routing, automatic protection switching, etc., may also be a source of phase variation.

4 Impairments caused by phase variation

4.1 *Types of impairments*

4.1.1 *Errors*

Errors may occur at points of signal regeneration as a result of timing signals being displaced from their optimum positions in time.

4.1.2 *Degradation of digitally encoded analogue information*

Degradation of digitally encoded analogue information may occur as a result of phase variation of the reconstructed samples in the digital to analogue conversion device at the end of the connection. This may have significant impact on digitally encoded video signals.

4.1.3 *Slips*

Slips arise as a result of the inability of an equipment buffer store (and/or other mechanisms) to accommodate differences between the phases and/or frequencies of the incoming and outgoing signals in cases where the timing of the outgoing signal is not derived from that of the incoming signal. Slips may be controlled or uncontrolled depending on the slip control strategy.

4.2 *Control of impairments*

4.2.1 *Errors*

The intent of both network and equipment jitter specifications is to ensure that jitter has no impact on the error performance of the network.

4.2.2 *Degradation of digitally encoded analogue signals*

The intent of jitter specifications is to provide sufficient information to enable equipment designers to accommodate the expected levels of phase variation without incurring unacceptable degradations.

4.2.3 *Slips*

Slips may occur in asynchronous multiplexes and various synchronous equipments. Given the specified levels of phase variation, slip occurrences may be minimised in asynchronous muldexes by appropriate choice of justification and muldex buffer capacity within. For synchronous equipments, slip occurrences may be minimised by appropriate choice of buffer capacity as well as rigorous specification of clock performance.

It should be noted that it is impossible to eliminate slips when there is a frequency difference between the incoming and outgoing timing signals. Controlled slip performance objectives for an international connection are given in Recommendation G.822.

Various forms of aligning equipment may be used to minimise the impact of slips. The following two forms of aligning equipment are suitable for the termination of digital signals:

— frame aligner ;

— time-slot aligner

4.2.3.1 Where a frame aligner is used, a slip will consist of the insertion or removal of a consecutive set of digits amounting to a frame. In the case of frame structures defined in Recommendation G.704 the slip can consist of one complete frame. It is of importance that the maximum and mean delays introduced by the frame aligner should be as small as possible in order to minimize delay. It is also of importance that, after the frame aligner has produced a slip, it should be capable of absorbing substantial further changes in the arrival time of the frame alignment signals before a further slip is necessary.

4.2.3.2 Where a slot aligner is used, a slip will consist of the insertion or removal of eight consecutive digit positions of a channel time slot in one or more 64 kbit/s channels. Because slips may occur on different channels at different times, special control arrangements will be necessary in switches if octet sequence integrity of multiple time-slot services is to be maintained.

5 **Purpose of phase variation specifications**

5.1 *Jitter*

Jitter requirements given in Recommendations G.823 and G.824 fall into two basic categories:

— specification of the maximum permissible jitter at the output of hierarchical interfaces;

— sinusoidal jitter stress test specifications to ensure the input ports can accommodate expected levels of network jitter.

Additional jitter requirements for individual equipments may be found in the appropriate equipment Recommendations.

5.2 *Wander and long term frequency departure*

Relevant wander requirements fall into the following categories:

i) maximum permissible wander at the output of synchronous network nodes;

ii) stress tests to ensure that synchronous equipment input ports can accommodate expected levels of network wander;

iii) wander specifications for primary reference and slave clocks may include:

a) intrinsic output wander under ideal conditions;

b) intrinsic output wander under free-running conditions;

c) output wander under stress test conditions;

d) wander transfer characteristic.

The purpose of these Recommendations is not only to provide limits for the allowance wander accumulation along the transmission paths but also for the wander accumulation along the synchronization distribution paths arising from cascaded clocks.

6 Structure of synchronization networks

6.1 *Synchronization modes*

International networks usually work in the plesiochronous mode one with another.

The synchronization of national networks may be of the following types:

— fully synchronized , controlled by one or several primary reference clocks;

— fully plesiochronous ;

— mixed, in which synchronized sub-networks are controlled by one or several primary reference clocks functioning plesiochronously one with another.

6.2 *Synchronization networks*

There are two fundamental methods of synchronizing nodal clocks:

— master-slave synchronization ;

— mutual synchronization

The master-slave synchronization system has a single primary reference clock to which all other clocks are phase-locked. Synchronization is achieved by conveying the timing signal from one clock to the next clock. Hierarchies of clocks can be established with some clocks being slaved from higher order clocks and in turn acting as master clocks for lower order clocks.

In a mutual synchronization system, all clocks are interconnected; there is no underlying hiearchical structure or unique primary reference clock.

Some practical synchronization strategies combine master-slave and mutual synchronization techniques.

Recommendation G.811

TIMING REQUIREMENTS AT THE OUTPUTS OF PRIMARY REFERENCE | fR CLOCKS SUITABLE FOR

PLESICHRONOUS OPERATION OF INTERNATIONAL DIGITAL LINKS

(Melbourne, 1988)

1 General

1.1 *International connections and network synchronization considerations*

National digital networks, which may have a variety of internal synchronization arrangements, will usually be connected by international links which operate plesiochronously. International switching centres (ISCs) will be interconnected directly or indirectly via one or more intermediate ISCs, as indicated in the hypothetical reference connection (HRX) shown in Figure 1/G.801.

International connections terminate on synchronous network nodes that may or may not be co-located with a primary reference clock. Such network nodes may include slave clocks. Therefore, synchronous network node clock specifications are essential to ensure satisfactory operation of plesiochronous international digital links.

Figure 1/G.811 illustrates the two alternative international connections described above.

Figure 1/G.811, p.

1.2 *Purpose of this Recommendation*

The purpose of this Recommendation is to specify requirements for primary reference clocks, promote understanding of associated timing requirements for plesiochronous operation of international digital links, and to clarify the relationship of the requirements for synchronous network nodes, constituent clocks and the use of satellite systems.

Administrations may apply this Recommendation, at their own discretion, to primary reference clocks other than those used in connection with international traffic.

1.3 *Interaction between plesiochronous and synchronous international operation*

It is important that the Recommendations for plesiochronous operation should not preclude the possibility of the later introduction of international synchronization.

When plesiochronous and synchronous operations coexist within the international network, the nodes will be required to provide for both types of operation. It is therefore important that the synchronization controls do not cause short-term frequency departures of the clocks which are unacceptable for plesiochronous operation. The magnitudes of the short-term frequency departures should satisfy the specifications in § 2.2.

1.4 *Maximum time interval error and relationship with frequency departure*

Maximum time interval error (MTIE) is the maximum peak-to-peak variation in the time delay of a given timing signal with respect to an ideal timing signal within a particular time period (Figure 2/G.811), i.e. MTIE(*S*) = max *x* (*t*)-min *x* (*t*) for all *t* within *S* .

Figure 2/G.811, p.

Long-term frequency departure (?63 *f* /*f*) is determined by the MTIE divided by the observation interval *S* , as *S* increases.

Note — The rigorous definition and measurement of long-term frequency departure for clocks is a subject for further study.

2 Long-term frequency departure and phase stability of primary reference clocks

A primary reference clock controls the synchronization performance of the overall network. It is necessary to specify the long-term frequency departure and phase stability of a primary reference clock, and to provide guidance concerning issues associated with degradation and unavailability performance. The definition of a primary reference clock is given in Recommendation G.810.

2.1 *Long-term frequency departure*

A primary reference clock should be designed for a long-term frequency departure of not greater than $1 \times 10^{\mathrm{D}}$lF261^{11}. The long-term frequency departure of $1 \times 10^{\mathrm{D}}$lF261^{11} is about two orders of magnitude larger than the uncertainty of Coordinated Universal Time (UTC). Therefore UTC should be the reference for long-term frequency departure (see CCIR Report 898).

The theoretical long-term mean rate of occurrence of controlled frame or octet slips (i.e. the design rate of slips based on ideally undisturbed conditions) in any 64 kbit/s channel is consequently not greater than one in 70 days per digital international link (see Recommendation G.822).

Note 1 — Some Administrations support a primary reference clock long-term frequency departure of not greater than $7 \times 10^{\mathrm{D}}$lF261^{12} based upon current primary reference clock technology.

Note 2 — Caesium-beam technology is suitable for primary reference clocks complying with the above specification.

2.2 *Phase stability*

The phase stability of a clock can be described by its phase variations, which in turn can be separated into a number of components:

— phase discontinuities due to transient disturbances;

— long-term phase variations (wander and integrated frequency departure);

— short-term phase variations (jitter).

A phase stability model for primary reference clocks is described in the annex to this Recommendation.

2.2.1 *Phase discontinuities*

Primary reference clocks need a very high reliability and are likely to include replication of the equipment in order to ensure the continuity of output. However, any phase discontinuity, due to internal operations within the clock, should only result in a lengthening or shortening of the timing signal interval and must not cause a phase discontinuity in excess of 1/8 of a unit interval at the clock output. (This refers to output signals at 1544 kbit/s or 2048 kHz, see § 4. Specification of other interfaces is under study.)

2.2.2 *Long-term phase variations*

The maximum permissible long-term phase variation of the output of a primary reference clock (whether sinusoidal or pulse) is expressed in MTIE.

The MTIE over a period of *S* seconds shall not exceed the following limits:

a) 100 *S* ns for the interval 0.05 < *S* 5

b) (5 *S* + 500) ns for the interval 5 < *S* 500

c) (0.01 *S* + *X* | ns for values of *S* > 500.

The asymptote designated 10^{D}lF261^{11} refers to the long-term frequency departure specified in § 2.1.

The value of *X* is under study. It is provisionally recommended that *X* = 3000 ns. Certain Administrations support a value of 1000 ns.

Note 1 — For measurement of long-term phase variations, the use of a 10 Hz low-pass filter is suggested.

Note 2 — The MTIE Recommendation requires further study.

Note 3 — The overall specification is illustrated in Figure 3/G.811.

2.2.3 *Short-term phase variations*

Clock implementations exist today which may have some high-frequency phase instability components. The specification of maximum permissible short- term phase variation of a primary reference clock due to jitter is under study.

3 Degradation of the performance of a primary reference clock

To achieve the required high reliability a primary reference clock includes redundancy, i.e. by incorporating several (caesium beam) oscillators, the output of only one of these being used at any given time. If a clock frequency departs significantly from its nominal value, this should be detected and switching to an undegraded oscillator should then be effected. This switching should be accomplished before the MTIE specification is exceeded.

With current technology, the performance of a primary reference clock is statistically well below the MTIE specification of Figure 3/G.811.

4 Interfaces

The preferred interface for the timing output is in accordance with Recommendation G.703, § 10, i.e. an interface at 2048 kHz. By agreement between operators or manufacturers of equipment, the timing signal may also be delivered at various other physical interfaces (e.g., 1544 kbitB/Fs primary rate signal, 1 MHz, 5 MHz, or 10 MHz).

5 Use of satellite systems in an international plesiochronous digital network

It is recommended that the link be operated in a plesiochronous mode using high accuracy (1×10^{D}lF261^{11}) source for the satellite TDMA timing. The international satellite links will be terminated on network nodes whose timing is in accordance with Recommendations G.823 and G.824.

Figure 3/G.811, p.9

6 Guidelines concerning the measurement of jitter and wander

Verification of compliance with jitter and wander specifications requires standardized measurement methodologies to eliminate ambiguities in the measurements and in interpretation and comparison of measurement results. Guidelines concerning the measurement of jitter and wander are contained in Supplement No. 3.8 (O-Series) and Supplement No. 35 at the end of this Fascicle.

ANNEX A

(to Recommendation G.811)

Characterization of primary reference clock phase stability

The following phase stability model may be employed to characterize primary reference clocks. Let $x(t)$ represent the time interval error of a clock synchronized at $t = 0$, and free-running against UTC thereafter. $x(t)$ may be defined as:

where:

D is the normalized linear frequency drift per unit time (ageing),

y_0 is the initial frequency departure with respect to UTC, and

$e(t)$ is the random error component.

The estimate of the standard deviation of $x(t)$ may be obtained, and used for characterization of phase instability.

where:

σ $$Ei:2:y _ is the two-sample variance of the initial frequency departure, and

σ $$Ei:2:y _ (τ) is the two-sample Allan variance describing the random frequency instability of the clock.

Recommendation G.812

TIMING REQUIREMENTS AT THE OUTPUTS OF SLAVE CLOCKS SUITABLE FOR PLESIOCHRONOUS OPERATION OF INTERNATIONAL DIGITAL LINKS

(Melbourne, 1988)

1 General

1.1 *Purpose of this Recommendation*

The purpose of this Recommendation is to specify requirements for slave clocks, and promote understanding of associated timing requirements for plesiochronous operation of international digital links.

Note — Administrations may apply this Recommendation, at their own discretion, to slave clocks other than those used in connection with international traffic. Supplement No. 35 gives guidance on one suitable method for the measurement of clock performance with respect to this Recommendation.

1.2 *Maximum relative time interval error*

The concept of maximum relative time interval error (MRTIE) is useful in specifying slave clock performance. MRTIE is analogous to MTIE as defined in Recommendation G.811 but with reference to a practical high-performance oscillator instead of UTC.

2 Phase stability of slave clocks

The phase stability of a slave clock can be described by its phase variations which in turn can be separated into a number of components:

— phase discontinuities due to transient disturbances;

— long-term phase variations (wander and integrated frequency departure);

— short-term phase variations (jitter).

A phase stability model for slave clocks is described in Annex A to this Recommendation.

2.1 *Phase discontinuity*

In cases of infrequent internal testing or rearrangement operations within the slave clock, the following conditions should be met:

— the phase variation over any period up to 2^{11} UI should not exceed 1/8 of a UI;

— for periods greater than 2^{11} UI in the phase variation for each interval or 2^{11} UI should not exceed 1/8 UI up to a total amount of 1 µs,

Where the UI corresponds to the reciprocal of the bit rate of the interface.

2.2 *Long-term phase variations*

Slave clock phase stability requirements must account for clock behaviour in real network environments. Impairments such as jitter, error bursts, and outages are intrinsic characteristics of timing distribution facilities. The following specifications are based on the slave clock phase stability model contained in the Annex. This model characterizes actual clock performance, reflecting the stress conditions in real networks under which clocks should perform acceptably. There are three categories of clock operation which require specification:

i) ideal,

ii) stressed, and

iii) holdover.

2.2.1 *Ideal operation*

This category of operation reflects the performance of a clock under conditions in which there are no impairments on the input timing reference(s).

The MRTIE at the output of the slave clock should not, over any period of *S* seconds, exceed the following provisional limits:

1) 0.05 < | fIS < | 00: this region requires further study;

2) 1000 ns for *S* ≥" | 00.

The resultant overall specification is summarized in Figure 1/G.812.

Figure 1/G.812, p.

2.2.2 *Stressed operation*

This category of operation reflects the actual performance of a clock considering the impact of real operating (stressed) conditions. Stressed conditions include the effects of jitter, protection switching activity, and error bursts. The result of such stressed conditions is timing impairments, as discussed in the Annex.

The requirements for stressed operation are under study.

2.2.3 *Holdover operation*

This category of operation reflects the performance of a clock for the infrequent times when a slave clock will lose reference for a significant period of time.

The MRTIE (see § 1.2 and Recommendation G.811) at the output of the slave clock should not, over any period of *S* seconds, exceed the following provisional limits.

For *S* ≥" 100, MRTIE | *S*) = (a*S* + 1/2 b*S* 2
+ *c*) ns

where parameters a, b, c are proposed provisionally in Table 1/G.812 (Note 5):

H.T. [T1.812]
TABLE 1/G.812

Transit node clock | ua) (stratum 2 clock) } Local node clock | ua) (stratum 3 clock) }	{ {	
a	0.5 (Note 1)	10.0 (Note 3)
b 1.16 × 10DlF261 5 (Note 2) } 2.3 × 10DlF261 4 (Note 4) }	{ {	
c 1000 (Note 6) }	1000 (Note 6)	{

a) See Recommendation G.810 for definitions.

Note 1 — Corresponds to un initial frequency offset of 5 × 10DlF261 10.

Note 2 — Corresponds to a frequency drift of 1 × 10DlF261 9/day.

Note 3 — Corresponds to an initial frequency offset of 1 × 10DlF261 8.

Note 4 — Corresponds to a frequency drift of 2 × 10DlF261 8/day.

Note 5 — Temperature effects: the effect of changes in environmental temperature on the performance of a slave clock in holdover mode requires further study.

Note 6 — Takes care of any MRTIE that might have existed at the beginning of holdover operation, and of effects of internal configuration, etc. in the clock (and timing distribution, if applicable). In any case, a smooth transition between ‘‘ideal’’ and ‘‘hold-over’’ operations is stipulated.

Tableau 1/G.812 [T1.812], p.

The resultant overall specification is summarized in Figure 2/G.812.

2.3 *Short-term phase variations*

Clock implementations exist which may have some high frequency phase instability components. The maximum permissible short-term phase variation of a slave clock due to jitter is under study.

Figure 2/G.812, p.12

ANNEX A
(to Recommendation G.812)

Characterization of slave clock phase stability

A.1 The slave clock model is described by the following equation:

where,

$x(t)$ is the phase-time output relative to the reference input (dimension time);

y b\di\da\ds is a residual fractional frequency offset which can arise from disruption events on the reference input (dimensionless);

D is the linear frequency drift component when the clock is in holdover condition (dimension 1/time);

$e_{p\backslash dm}(t)$ is a white noise phase modulation (PM) component associated with the short-term instability of the clock (dimension time);

$e_{f\backslash dm}(\tau)$ is a white noise fractional frequency modulation (FM) component associated with the disruption process of the reference (dimensionless).

The clock model is best understood by considering the three categories of clock operation:

— ideal operation;

— stressed operation;

— holdover operation.

A.1.1 *Ideal operation*

For short observation intervals outside the tracking bandwidth of the PLL, the stability of the output timing signal is determined by the short term stability of the local synchronizer time base. In the absence of reference disruptions, the stability of the output timing signal behaves asymptotically as a white noise PM process as the observation period is increased to be within the tracking bandwidth of the PLL. The output of the clock can be viewed as a superposition of the high frequency noise of the local oscillator riding on the low frequency portion of the input reference signal. In phase locked operation the high frequency noise must be bounded, and is uncorrelated (white) for large observation periods relative to the bandwidth of the phase locked loop.

Under ideal conditions, the only non-zero parameter of the model is the white noise PM component.

A.1.2 *Stressed operation*

In the presence of interruptions, the stability of the output timing signal behaves as a white noise FM process as the observation period is increased to be within the tracking bandwidth of the PLL. The presence of white noise FM can be justified based on the simple fact that in general, network clocks extract time interval, rather than absolute time from the time reference. An interruption is by nature a short period during which the reference time interval is not available. When reference is restored there is some ambiguity regarding the actual time difference between the local clock and the reference. Depending on the sophistication of the clock phase build-out there can be various levels of residual phase error which occur for each interruption. There is a random component which is independent from one interruption event to the next which results in a random walk in phase, i.e. a white noise FM noise source.

In addition to the white noise FM component, interruption events can actually result in a frequency offset between the clock and its reference. This frequency offset ($y_{b\backslash di\backslash da\backslash ds}$) results from a bias in the phase build-out when reference is restored. This is a critical point. The implications of this effect are that in actual network environments there is some accumulation of frequency offset through a chain of clocks. Thus, clocks controlled by the same primary reference clock are actually operating plesiochronously to some degree.

To summarize, under stress conditions the non-zero parameters of the clock model are the white noise FM component ($e_{f\backslash dm}$) and the frequency offset component ($y_{b\backslash di\backslash da\backslash ds}$). The stressed category of operation reflects a realistic characterization of what ‘‘normal’’ operation of a clock is.

A.1.3 *Holdover operation*

In holdover, the key components of the clock model are the frequency drift (D) and the initial frequency offset ($y_{b\backslash di\backslash da\backslash ds}$). The drift term accounts for the significant ageing associated with quartz oscillators. The initial frequency offset is associated with the intrinsic setability of the local oscillator frequency.

A.2 *Relationship of slave clock model to TIE performance*

It is useful to consider the relationship between the clock model and the Time Interval Error (TIE) that would be expected. It is proposed that the two sample Allan variance be used to describe the stochastic portion of the clock model. The following equations apply for the three categories of operation:

Ideal

Stressed

Holdover

where,

$\sigma_{T\backslash dI\backslash dE}$ is the standard deviation of the relative time interval error of the clock output compared to the reference over the observation time *t* ;

$\sigma, (\tau)$ is the two sample standard deviation describing the random frequency fluctuation of the clock, and

$\sigma_{b\backslash di\backslash da\backslash ds}$ describes the two sample standard deviation of the frequency bias.

A.3. *Guidelines concerning the measurement of jitter and wander*

Verification of compliance with jitter and wander specifications requires standardized measurement methodologies to eliminate ambiguities in the measurements and in the interpretation and comparison of measurement results. Guidance concerning the measurement of jitter and wander is contained in Supple ment No. 35.

MONTAGE: DEBUT DE REC. G.821 A LA FIN DE CETTE PAGE