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Recommendation G.704

SYNCHRONOUS FRAME STRUCTURES USED AT PRIMARY AND SECONDARY HIERARCHICAL LEVELS

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

1 General

This Recommendation gives functional characteristics of interfaces associated with:

— network nodes, in particular, synchronous digital multiplex equipment and digital exchanges in IDNs for telephony and ISDNs, and

— PCM multiplexing equipment.

Paragraph 2 deals with basic frame structures, including details of frame length, frame alignment signals, cyclic redundancy check (CRC) procedures and other basic information.

Paragraphs 3 to 6 contain more specific information about how certain channels at 64 kbit/s and at other bit rates are accomodated within the basic frame structures described in § 2.

Electrical characteristics for these interfaces are defined in Recommendation G.703.

Note 1 — This Recommendation does not necessarily apply to those cases where the signals that cross the interfaces are devoted to non-switched connections, such as those for the transport of encoded wideband signals (e.g. broadcast TV signals or multiplexed sound-programme signals which need not be individually routed via the ISDN), see also Annex A to Recommendation G.702.

Note 2 — The frame structures recommended in this Recommendation do not apply to certain maintenance signals, such as the all 1s signals transmitted during fault conditions or other signals transmitted during out-of-service conditions.

Note 3 — Frame structures associated with digital multiplexing equipments using justification are covered in each corresponding equipment Recommendation.

Note 4 — Inclusion of channel structures at other bit rates than 64 kbit/s is a matter for further study. Recommendations G.761 and G.763 dealing with the characteristics of PCM/ADPCM transcoding equipment contain information about channel structures at 32 kbit/s. The more general use of those particular structures is a subject of further study.

2 Basic frame structures

2.1 *Basic frame structure at 1544 kbit/s*

2.1.1 *Frame length* :

193 bits, numbered 1 to 193. The frame repetition rate is 8000 Hz.

2.1.2 *F-bit*

The first bit of a frame is designated an F-bit, and is used for such purposes as frame alignment, performance monitoring and providing a data link.

2.1.3 *Allocation of F-bit*

Two alternative methods as given in Tables 1/G.704 and 2/G.704 for allocation of F-bits are recommended.

H.T. [T1.704]

TABLE 1/G.704

Multiframe structure for the 24 frame multiframe

{		{ Assignements FAS {	DL	{			
1	1	—	*m*	—	1-8	—	.
2	194	—	—	*e* 1	1-8	—	.
3	387	—	*m*	—	1-8	—	.
4	580	0	—	—	1-8	—	.
5	773	—	*m*	—	1-8	—	.
6	966	—	—	*e* 2	1-7	8	A
7	1159	—	*m*	—	1-8	—	.
8	1352	0	—	—	1-8	—	.
9	1545	—	*m*	—	1-8	—	.
10	1738	—	—	*e* 3	1-8	—	.
11	1931	—	*m*	—	1-8	—	.
12	2124	1	—	—	1-7	8	B
13	2317	—	*m*	—	1-8	—	.
14	2510	—	—	*e* 4	1-8	—	.
15	2703	—	*m*	—	1-8	—	.
16	2896	0	—	—	1-8	—	.
17	3089	—	*m*	—	1-8	—	.
18	3282	—	—	*e* 5	1-7	8	C
19	3475	—	*m*	—	1-8	—	.
20	3668	1	—	—	1-8	—	.
21	3861	—	*m*	—	1-8	—	.
22	4054	—	—	*e* 6	1-8	—	.
23	4247	—	*m*	—	1-8	—	.
24	4440	1	—	—	1-7	8	D

FAS Frame alignement signal (. | | 001011 . | |).

DL 4 kbit/s data link (message bits *m*).

CRC CRC-6 (block check field (check bits *e* 1 . | | *e* 6).

a) Only applicable in the case of channel associated signalling see (§ 3.1.3.2.)

Tableau 1/G.704 [T1.704], p. 1

H.T. [T2.704]

TABLE 2/G.704

Allocation of F-bit for the 12-frame multiframe

Tableau 2/G.704 [T2.704], p. 2

2.1.3.1 *Method 1: Twenty-four-frame multiframe*

Allocation of the F-bit to the multiframe alignment signal, the CRC check bits and the data link is given in Table 1/G.704.

2.1.3.1.1 *Multiframe alignment signal*

The F-bit of every fourth frame forms the pattern 001011 . | | 001011. This multiframe alignment signal is used to identify where each particular frame is located within the multiframe in order to extract the cyclic redundancy check code, CRC-6, and the data link information, as well as to identify those frames that contain signalling (frames 6, 12, 18 and 24), if channel associated signalling is used.

2.1.3.1.2 *Cyclic redundancy check*

The CRC-6 is a method of performance monitoring that is contained within the F-bit position of frames 2, 6, 10, 14 18 and 22 of every multiframe (see Table 1/G.704).

The CRC-6 message block check bits e_1, e_2, e_3, e_4, e_5, and e_6 are contained within multiframe bits 194, 966, 1738, 2510, 3282 and 4054 respectively, as shown in Table 1/G.704. The CRC-6 Message Block (CMB) is a sequence of 4632 serial bits that is coincident with a multiframe. By definition, CMB *N* begins at bit position 1 of multiframe *N* and ends at bit position 4632 of multiframe *N* . The first transmitted CRC bit of a multiframe is the most significant bit of the CMB polynomial.

In calculating the CRC-6 bits, the F-bits are replaced by binary 1s. All information in the other bit positions will be identical to the information in the corresponding multiframe bit positions.

The check-bit sequence e_1 through e_6 transmitted in multiframe N +1, is the remainder after multiplication by x^6 and then division (modulo-2) by the generator polynomial $x^6 + x + 1$ of the polynomial corresponding to CMB *N* . The first check bit (e_1) is the most significant bit of the remainder; the last check bit

(e_6) is the least significant bit of the remainder. Each multiframe contains the CRC-6 check bits generated for the preceding CMB.

At the receiver, the received CMB, with each F-bit having first been replaced by a binary 1, is acted upon by the multiplication/division process described above. The resulting remainder is compared on a bit-by-bit basis, with the CRC-6 check bits contained in the subsequently received multiframe. The compared check bits will be identical in the absence of transmission errors.

2.1.3.1.3 *4 kbit/s data link*

Beginning with frame 1 of the multiframe (see Table 1/G.704) the first bit of every other frame is part of the 4 kbit/s data link. This data link provides a communication path between primary hierarchical level terminals and will contain data, an idle data link sequence or a loss of frame alignment alarm sequence.

The format to be used for the transmission of data over the *m* -bits of the data link is still under study.

The idle data link pattern is also under study.

A loss of frame alignment alarm sequence is used when a loss of frame alignment (LFA) condition has been detected. After a loss of frame alignment condition is detectd at local end A, a 16-bit LFA sequence of eight 1s eight 0s (1111111100000000) will be transmitted in the *m* -bits of the 4 kbit/s data link continuously to remote end B.

2.1.3.2 *Method 2: Twelve-frame multiframe*

Allocation of the F-bit to the frame alignment signal, multiframe alignment signal and signalling is given in Table 2/G.704.

2.2 *Basic frame structure at 6312 kbit/s*

2.2.1 *Frame length*

The number of bits per frame is 789. The frame repetition rate is 8000 Hz.

2.2.2 *F-bits*

The last five bits of a frame are designated as F-bits, and are used for such purposes as frame alignment, performance monitoring and providing a data link.

2.2.3 *Allocation of F-bits*

Allocation of the F-bits is given in Table 3/G.704.

[T3.704] **Table 3/G.704 [T3.704], p.**

2.2.3.1 *Frame alignment signal*

The frame and multiframe alignment signal is 110010100, and is carried on the F-bits in frames 1 and 2, excluding bit 789 of frame 1.

2.2.3.2 *Cyclic redundancy check*

The cyclic redundancy check 5 (CRC-5) message block (CMB) is a sequence of 3151 serial bits which starts at bit number 1 of frame number 1 and ends at bit number 784 of frame number 4. The CRC-5 message block check bits e_1, e_2, e_3, e_4 and e_5 occupy the last five bits of the multiframe as shown in Table 3/G.704.

The check-bit sequence e_1 through e_5 transmitted in multiframe N is the remainder after multiplication by x^5 and then division (modulo-2) by the generator polynomial $x^5+x^4+x^2+1$ of the polynomial corresponding to CMB N. The first check bit (e_1) is the most significant bit of the remainder; the last check bit (e_5) is the least significant bit of the remainder. Each multiframe contains the CRC-5 check bits generated for the corresponding CMB.

At the receiver the incoming sequence of 3156 serial bits (i.e. 3151 bits of CMB and 5 CRC bits), when divided by the generator polynomials, will result in a remainder of 00000 in the absence of transmission errors.

2.2.3.3 *4 kbit/s data link*

The bit *m* shown in Table 3/G.704 is used as a data link bit. These bits provide 4 kbit/s data transmission capability associated with the 6312 kbit/s digital path.

2.2.3.4 *Remote end alarm indication*

After a loss of frame alignment condition is detected at local end A, remote end alarm signal bit *a* , shown in Table 3/G.704, will be transmitted to remote end B.

2.3 *Basic frame structure at 2048 kbit/s*

2.3.1 *Frame length*

256 bits, numbered 1 to 256. The frame repetition rate is 8000 Hz.

2.3.2 *Allocation of bits number 1 to 8 of the frame*

Allocation of bits number 1 to 8 of the frame is shown in Table 4a/G.704.

[T4.704] **Table 4a/G.704 [T4.704], p.**

2.3.3 *Description of the CRC-4 procedure in bit 1 of the frame*

2.3.3.1 *Special use of bit 1 of the frame*

Where there is a need to provide additional protection against simulation of the frame alignment signal, and/or where there is a need for an enhanced error monitoring capability, then bit 1 should be used for a Cyclic Redundancy Check-4 (CRC-4) procedure as detailed below.

Note — Equipment incorporating the CRC-4 procedure should be designed to be capable of interworking with equipment which does not incorporate the CRC procedure, with the option being manually selectable (e.g. by straps). For such interworking, bit 1 of the frame should be fixed at 1 in both directions (see Table 4a/G.704, Note 1).

2.3.3.2 The allocation of bits 1 to 8 of the frame is shown in Table 4b/G.704 for a complete CRC-4 multiframe.

[T5.704] **Table 4b/G.704 [T5.704], p.**

2.3.3.3 Each CRC-4 multiframe, which is composed of 16 frames numbered 0 to 15, is divided into two 8-frame sub-multiframes (SMF), designated SMF I and SMF II which signifies their respective order of occurrence within the CRC-4 multiframe structure. The SMF is the Cyclic Redundancy Check-4 (CRC-4) block size (i.e. 2048 bits).

The CRC-4 multiframe structure is not related to the possible use of a multiframe structure in 64 kbit/s channel time slot 16 (see § 5.1.3.2).

2.3.3.4 *Use of bit 1 in 2048 kbit/s CRC-4 multiframe*

In those frames containing the frame alignment signal (defined in § 2.3.2), bit 1 is used to transmit the CRC-4 bits. There are four CRC-4 bits, designated C_1, C_2, C_3 and C_4 in each SMF.

In those frames not containing the frame alignment signal (see § 2.3.2), bit 1 is used to transmit the 6-bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E).

The CRC multiframe alignment signal has the form 001011.

The E-bits should be used to indicate received errored sub-multiframes by setting the binary state of one E-bit from 1 to 0 for each errored sub-multiframe. Any delay between the detection of an errored sub-multiframe and the setting of the E-bit that indicates the error state must be less than 1 second.

Note 1 — The E-bits will always be taken into account even if the SMF which contains them is found to be errored, since there is little likelihood that the E-bits themselves will be errored.

Note 2 — In the short term, there may exist equipments which do not use the E-bits; in this case the E-bits are set to binary 1.

2.3.3.5 *Cyclic Redundancy Check*

2.3.3.5.1 *Multiplication/division process*

A particular CRC-4 word, located in sub-multiframe N, is the remainder after multiplication by x^4 and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of sub- multiframe N | (em |).

Note — When representing the contents of the check block as a polynomial, the first bit in the block, i.e. frame 0, bit 1 or frame 8, bit 1, should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_4 the least significant bit of the remainder.

2.3.3.5.2 *Encoding procedure*

i) The CRC-4 bits in the SMF are replaced by binary 0s.

ii) The SMF is then acted upon by the multiplication/division process referred to in § 2.3.3.5.1.

iii) The remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

Note — The CRC-4 bits thus generated do not affect the result of the multiplication/division process in the next SMF because, as indicated in i) above, the CRC-4 bit positions in an SMF are initially set to 0 during the multiplication/division process.

2.3.3.5.3 *Decoding procedure*

i) A received SMF is acted upon by the multiplication/division process referred to in § 2.3.3.5.1, after having its CRC-4 bits extracted and replaced by 0s.

ii) The remainder resulting from this division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.

iii) If the remainder calculated in the decoder exactly corresponds to the CRC-4 bits received in the next SMF, it is assumed that the checked SMF is error free.

2.4 *Basic frame structure at 8448 kbit/s*

2.4.1 *Frame length*

The number of bits per frame is 1056. They are numbered from 1 to 1056. The frame repetition rate is 8000 Hz.

2.4.2 *Frame alignment signal*

The frame alignment signal is 11100110 100000 and occupies the bit-positions 1 to 8 and 529 to 534.

2.4.3 *Service digits*

Bit 535 is used to convey alarm indication (bit 535 at 1 state — alarm; bits 535 at 0 state = no alarm).

Bit 536 is left free for national use and should be fixed at 1 on paths crossing the international border. The same applies to bits 9-40 in the case of channel-associated signalling.

3 Characteristics of frame structure carrying channels at various bit rates in 1544 kbit/s

3.1 *Interface at 1544 kbit/s carrying 64 kbit/s channels*

3.1.1 *Frame structure*

3.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

3.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 2 to 193 in the basic frame carry 24 octet interleaved 64 kbit/s channel time slots, numbered 1 to 24.

3.1.1.3 *Allocation of F-bit*

Refer to § 2.1.3.

3.1.2 *Use of 64 kbit/s channel time slots*

Each 64 kbit/s channel time slot can accommodate e.g., a PCM encoded voiceband signal conforming to Rec. G.711 or data information with a bit rate up to 64 kbit/s.

3.1.3 *Signalling*

Two alternative methods as given in §§ 3.1.3.1 and 3.1.3.2 are recommended:

3.1.3.1 *Common channel signalling*

One 64 kbit/s channel time slot is used to provide common channel signalling at a rate of 64 kbit/s. In the case of the 12-frame multiframe method of § 2.1.3.2, the pattern of the S-bit may be arranged to carry common channel signalling at a rate of 4 kbit/s or a sub-multiple of this rate.

3.1.3.2 *Channel associated signalling*

3.1.3.2.1 *Allocation of signalling bits for the 24-frame multiframe*

As can be seen in Table 1/G.704, there are four different signalling bits (A, B, C and D) in the multiframe. This channel associated signalling can provide four independent 333-bit/s signalling channels designated A, B, C and D, two independent 667-bit/s signalling channels designated A and B (see Note,) or one 1333-bit/s signalling channel.

Note — When only four state signalling is required, the A, B signalling bits previously associated with frames 6 and 12 respectively should be mapped into the A, B, C, D signalling bits of frames 6, 12, 18 and 24 respectively as follows: A=A, B=B, C=A, D=B.

In this case the ABCD signalling is the same as the AB signalling specified in § 3.1.3.2.2.

3.1.3.2.2 *Allocation of signalling bits for the 12-frame multiframe*

Based on agreement between the Administrations involved, channel-associated signalling is provided for intra-regional circuits according to the following arrangement:

A multiframe comprises 12 frames as shown in Table 5/G.704. The multiframe alignment signal is carried on the S-bit as shown in the table.

Frames 6 and 12 are designated as signalling frames. The eight bit in each channel time slot is used in every signalling frame to carry the signalling associated with that channel.

[T6.704] **Table 5/G.704 [T6.704], p.**

3.2 *Interface at 1544 kbit/s carrying 32 kbit/s channel time slots* (see Note)

Note — This interface provides for the carrying of 32 kbit/s information. The interface will be used between network nodes and will apply to primary rate multiplexing equipment, digital cross-connect equipment, transcoder and other equipment relevant to the network nodes. Switching in this case is assumed to take place on a 64 kbit/s basis.

3.2.1 *Frame structure*

3.2.1.1 *Number of bits per 32 kbit/s channel time slot*

Four, numbered 1 to 4.

3.2.1.2 *Number of 32 kbit/s channel time slots per frame*

Bits 2 to 193 in the basic frame can carry forty-eight 4-bit interleaved 32 kbit/s channel time slots, numbered 1 to 48.

3.2.1.3 *Allocation of F-bits*

Refer to § 2.1.3.

3.2.2 *Use of 32 kbit/s channel time slot*

Each 32 kbit/s channel time slot can accomodate an ADPCM-encoded voiceband signal conforming to Rec. G.721, or data with a bit rate up to 32 kbit/s.

3.2.3 *384 kbit/s 12-channel time slot grouping*

3.2.3.1 *Structure of 12-channel time slot grouping*

The 1544 kbit/s frame for 32 kbit/s channel time slots shown in Table 6/G.704 is structured to provide four independent 384 kbit/s 12-channel time slot groupings. These are numbered 1-4, and transmitted in numbered order starting with time slot grouping number 1.

The signalling grouping channels (SGC) for time slot groupings 1-4, occupy time slots 12, 24, 36 and 48 respectively. Each time slot grouping can be independently configured for situations requiring channel associated signalling or situations with no signalling requirement (e.g. external common signalling). (See § 3.2.3.1.1.)

[T7.704] **Table 6/G.704 [T7.704], p.**

3.2.3.1.1 *Use of a 384 kbit/s time slot grouping*

Use of a 384 kbit/s time slot grouping is categorized into two possible configurations:

— When no signalling capabilities are required, a 384 kbit/s time slot grouping can carry twelve 32 kbit/s channel time slots;

— When channel associated signalling capabilities are required, a 384 kbit/s time slot grouping will consist of eleven 32 kbit/s channel time slots and a 32 kbit/s channel time slot defined as a signalling grouping channel.

3.2.3.1.2 *Use of a signalling grouping channel*

A signalling grouping channel is used for the transmission of channel associated A-B-C-D signalling information, signalling grouping channel alarm information, the signalling grouping channel multiframe alignment signal, and CRC-6 error detection information between network nodes.

3.2.4 *32 kbit/s signalling grouping channel multiframe structure*

3.2.4.1 *Number of bits per 32 kbit/s signalling grouping channel time slot*

Four, numbered 1 to 4.

3.2.4.2 *Bit allocation of 32 kbit/s signalling grouping channel time slot*

Allocated to the last four bits of each time slot grouping.

3.2.4.3 *Multiframe structure*

The signalling grouping channel multiframe structure consists of 24 consecutive frames numbered 1 to 24. Table 7/G.704 shows the signalling grouping channel multiframe structure.

[T8.704] **Table 7/G.704 [T8.704], p.**

3.2.4.4 *Signalling grouping channel multiframe alignment signal*

Bit 3 of the signalling grouping channel, as shown in Table 7/G.704, contains the signal grouping channel multiframe alignment signal used to associate the signalling bits in the signal grouping channel with the proper channels of the associated time slot grouping.

Note — The signalling grouping channel multiframe alignment signal is independent of, and different from, the framing bit of the 1544 kbit/s frame.

3.2.4.5 *CRC-6 error detection information for the time slot grouping*

An optional 2 kbit/s CRC-6 error detection code word may be transmitted in the bit position indicated by CRC-1 through CRC-6 in Table 7/G.704.

The CRC-6 message block (CMB) is a sequence of 1152 serial bits that is concident with a time slot grouping multiframe. By definition, CMB *N* begins at bit position 0 of time slot grouping multiframe *N* and ends at bit position 1151 of time slot grouping multiframe *N* .

The check-bit sequence CRC-1 through CRC-6 transmitted in multiframe $N+1$ is the remainder after multiplication by x^6, and then division (modulo 2) by the generator polynomial $x^6 + x + 1$ of the the polynomial corresponding to CMB *N* . The first check bit, CRC-1, is the most significant bit of the remainder; the last check bit CRC-6, is the least significant bit. The time slot grouping channel is included in this calculation with bit 4 of the time slot grouping channel being set to 1.

When not utilizing the option to transmit the CRC-6 error detection signal, CRC-1 through CRC-6 shall be set to 1.

3.2.4.6 *Signalling*

Two alternative methods as given in §§ 3.2.4.6.1 and 3.2.4.6.2 are recommended.

3.2.4.6.1

Refer to § 3.1.3.1. Two successive 32 kbit/s channel time slots are used for 64 kbit/s common channel signalling transmission.

3.2.4.6.2 *Channel associated signalling*

As indicated in Table 7/G.704, bits 1 and 2 of the signalling grouping channel convey the channel associated signalling information for the channels of the associated time slot grouping.

The signalling grouping channel can provide four independent 333 bit/s signalling channels designated A, B, C and D, two independent 667 bit/s signalling channels designated A and B, or one 1333 bit/s signalling channel designated A. Where only A-B signalling is used, the A-B signalling is repeated for the C-D positions respectively. Where only A signalling is used, the A signalling is repeated for the B-C-D positions respectively.

3.2.4.7 *Signalling grouping channel alarm indication signals*

As indicated in Table 7/G.704, the signalling grouping channel contains four alarm indication bits, M_1, M_2, M_3 and M_4.

M_1 provides the capability to transmit through the interface a remote time slot grouping alarm indication of a failure in the opposite direction of transmission.

M_2 provides the capability to transmit through the interface an indication of a failure in tributary input signals to the network node.

M_3 provides the capability to transmit through the interface an indication of a failure in tributary output signals from the network node.

M_4 is set to 1 whenever M_1 and/or M_2 and/or M_3 are set to 1.

3.2.5 *Signal grouping channel unused bits*

The bits marked S in Table 7/G.704 are currently unused and set to 1. The definition and allocation of the S-bits are for further study.

3.2.6 *Loss and recovery of signalling channel multiframe alignment*

Loss of the signalling grouping channel multiframe alignment signal is declared when two out of four signalling grouping channel framing bits are in error. The rare occurrence of a single instantaneous slip of ± | 1 frames is undetected by the two-out-of-four algorithm. Signalling grouping channel multiframe alignment shall be declared when the correct sequence of 24 valid signalling grouping channel framing bits is detected, beginning with the first frame of the multiframe.

3.3 *Interface at 1544 kbit/s carrying n × 64 kbit/s*

Electrical characteristics should follow Recommendation G.703.

The time slot mapping to the 1544 kbit/s interface is for further study.

4 Characteristics of frame structures carrying channels at various bit rates in 6312 kbit/s interfaces

4.1 *Interface at 6312 kbit/s carrying 64 kbit/s channels*

4.1.1 *Frame structure*

4.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

4.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 1 to 784 in the basic frame carry 98 octet interleaved 64 kbit/s channel time slots, numbered 1 to 98. Five bits per frame (F-bits) are added at the end of the frame for the frame alignment signal and for other signals.

4.1.1.3 *Allocation of the F-bits*

Refer to Table 3/G.704.

4.1.2 *Use of 64 kbit/s channel time slots*

Each 64 kbit/s channel time slot can accomodate e.g., a PCM-encoded voiceband signal conforming to Recommendation G.711 or data information with a bit rate up to 64 kbit/s. 64 kbit/s channel time slots 97, 98 may be used for signalling.

4.1.3 *Signalling*

Two alternative methods as given in §§ 4.1.3.1 and 4.1.3.2 are recommended.

4.1.3.1 *Common channel signalling*

Use of 64 kbit/s channel time slots 97 and 98 for common channel signalling is under study.

4.1.3.2 *Channel associated signalling*

Based on agreement between the Administrations concerned, channel associated signalling is provided for intra-regional circuits according to the following arrangement:

4.1.3.2.1 *Allocation of signalling bit*

Sixteen signalling bits (bit positions 769 to 784) are designated as ST_1 to $ST_{1\backslash d6}$. One ST_i-bit (i = 1 to 16) accomodates signalling information corresponding to six channel time slots i , 16 + i , 32 + i , 48 + i , 64 + i and 80 + i in a manner described in § 4.1.3.2.2 below.

4.1.3.2.2 *Signalling multiframe structure*

Each ST-bit constitutes an independent signalling multiframe over eight frames as shown in Table 8/G.704.

[T9.704] **Table 8/G.704 [T9.704], p.**

4.2 *Interfaces at 6312 kbit/s carrying other channels than 64 kbit/s*

For further study.

5 Characteristics of frame structures carrying channels at various bit rates in 2048 kbit/s interfaces

5.1 *Interface at 2048 kbit/s carrying 64 kbit/s channels*

5.1.1 *Frame structure*

5.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

5.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 1 to 256 in the basic frame carry 32 octet interleaved time slots numbered 0 to 31.

5.1.1.3 *Allocation of the bits of 64 kbit/s channel time slot 0*

See Table 4a/G.704 (§ 2.3.2).

5.1.2 *Use of other 64 kbit/s channel time slots*

Each of the 64 kbit/s channel time slots 1 to 15 and 17 to 31 can accomodate e.g., a PCM-encoded voiceband signal according to Recommendation G.711 or a 64 kbit/s digital signal.

The 64 kbit/s channel time slot 16 may be used for signalling. If not needed for signalling, in some cases it may be used for a 64 kbit/s channel in the same way as time slots 1 to 15 and 17 to 31.

5.1.3 *Signalling*

The use of 64 kbit/s channel time slot 16 is recommended for either common channel or channel associated signalling as required.

The detailed requirements for the organization of particular signalling systems will be included in the specifications for those signalling systems.

5.1.3.1 *Common channel signalling*

The 64 kbit/s channel time slot 16 may be used for common channel signalling systems up to a rate of 64 kbit/s. The method of obtaining signal alignent will form part of the particular common channel signallling specification.

5.1.3.2 *Channel associated signalling*

This section contains the recommended arrangement for the use of the 64 kbit/s capability of channel time slot 16 for channel associated signalling.

5.1.3.2.1 *Multiframe structure*

A multiframe comprises 16 consecutive frames (whose structure is given in § 5.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of 64 kbit/s channel time slot 16 in frame 0.

5.3.1.2.2 *Allocation of 64-kbit/s channel time slot 16*

When 64 kbit/s channel time slot 16 is used for channel associated signalling, the 64-kbit/s capacity is sub-multiplexed into lower-rate signalling channels using the multiframe alignement signal as a reference.

Details of the bit allocation are given in Table 9/G.704.

5.2 *Interface at 2048 kbit/s carrying $n \times 64$ kbit/s*

Electrical characteristics should follow Recommendation G.703 (see Note 4 of Preamble to G.703). For the accomodation of $n \times 64$ kbit time slots in the 2048 kbit/s frame, two situations are envisaged.

5.2.1 *One $n \times 64$ kbit/s signal on the tributary side of a multiplex equipment*

Time slots of the 2048 kbit/s frame are filled as follows:

TS0: according to § 2.3;

TS16: reserved for the accomodation, if required, of a 64 kbit/s signalling channel.

— If 2 | fIn | 15, TS1 to TS*n* are filled with $n \times 64$ kbit/s data [see a) of Figure 1/G.704];

— If 15 < *n* | 0, TS1 to TS15 and TS17 to TS(*n* +1) are filled with $n \times 64$ kbit/s data [see b) of Figure 1/G.704].

— Remaining time slots are filled with all 1s.

[T10.704] **Table 9/G.704 [T10.704], p.**

Figure 1/G.704, p.

5.2.2 *One or more $n \times 64$ kbit/s signal on the multiplexed signal side of a multiplexing equipment*

For any one $n \times 64$ kbit/s signal, time slots of the 2048 kbit/s frame are filled as follows:

TS0: according to § 2.3;

TS16: reserved for the accomodation, if required, of a 64 kbit/s signalling channel.

TS(x) of the 2048 kbit/s frame is designated as the time slot into which the first time slot of the $n \times 64$ kbit/s is accomodated.

— If x | 5 and $x + (n — 1)$ | 5, or, if x ≥" | 7 and $x + (n — 1)$ | 1, then the filling of time slots is from TS | x) to TS | $x + n$ —1) [see a)and b) of Figure 2/G.704];

— If $x + (n — 1)$ ≥" | 6, then the filling of time slots is from TS | x) to TS15 and TS17 to TS | $x + n$) (see c) of Figure 2/G.704).

Note — Once $n \times 64$ kbit/s signal has been accomodated into the multiplexed signal, care should be taken in the interpretation of the above rules to ensure that further such signals only use the time slots which remain spare.

Figure 2/G.704, p.

6 Characteristics of frame structures carrying channels at various bit rates in 8448 kbit/s interface

6.1 *Interface at 8448 kbit/s carrying 64 kbit/s channels*

6.1.1 *Frame structure*

6.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered from 1 to 8.

6.1.1.2 *Number of 64 kbit/s channel time time slots per frame*

Bits 1 to 1056 in the basic frame carry 132 octet interleaved 64 kbit/s channel time slots, numbered form 0 to 131.

6.1.2 *Use of 64 kbit/s channel time slots*

6.1.2.1 *64 kbit/s channel time slot assignment in case of channel associated signalling*

64 kbit/s channel time slots 5 to 32, 34 to 65, 71 to 98 and 100 to 131 are assigned to 120 telephone channels from 1 to 120.

64 kbit/s channel time slot 0 and the first 6 bits in 64 kbit/s channel time slot 66 are assigned to framing: the remaining 2 bits in 64 kbit/s channel time slot 66 are devoted to services.

64 kbit/s channel time slots 67 to 70 are assigned to channel associated signalling as covered in § 6.1.4.2 below.

64 kbit/s channel time slots 1 to 4, 33 are left free for national use.

6.1.2.2 *64 kbit/s channel time slot assignment in case of common channel signalling*

64 kbit/s channel time slots 2 to 32, 34 to 65, 67 to 98 and 100 to 131 are available for 127 telephone, signalling or other service channels. By bilateral agreement between the Administrations concerned, 64 kbit/s channel time slot 1 may either be used to provide another telephone or service channel or left free for service purposes within a digital exchange.

The 64 kbit/s channels corresponding to 64 kbit/s channel time slot 1 to 32, 34 to 65 (etc. as above) are numbered 0 to 127.

64 kbit/s channel time slot 0 and the first 6 bits in channel time slot 66 are assigned to framing, the remaining 2 bits in 64 kbit/s channel time slot 66 are assigned to service.

64 kbit/s channel time slots 67 to 70 are, in descending order of priority, available for common channel signalling as covered in § 6.1.4.1 below.

64 kbit/s channel slot 33 is left free for national use.

6.1.3 *Description of the CRC procedure in 64 kbit/s channel time slot 99*

In order to provide an end-to-end quality monitoring of the 8 Mbit/s link, a CRC-6 procedure is used and the six bits C_1 to C_6 computed at the source location are inserted in bit positions 1 to 6 of the time slot 99 (see Figure 3/G.704).

In addition, bit 7 of this time slot, denoted E, is used to send in the transmitting direction an indication about the received signal arriving from the opposite direction. Bit E indicates whether or not the most recent CRC block arriving at the opposite end had errors.

The CRC-6 bits C_1 to ${}_6$ are computed for each frame. The CRC-6 block size is then 132 octets, i.e. 1056 bits, and the computation is made 8000 times per second.

Figure 3/G.704, p.

6.1.3.1 *Multiplication/division process*

A given C_1-C_6 word located in frame *N* is the remainder after multiplication by x^6 and then division (modulo 2) by the generator polynomial $x^6 + x + 1$ of the polynomial representation of frame (*N* —1).

Note — When representing the contents of a frame as a polynomial, the first bit in the frame should be taken as being the most significant bit. Similarly C_1 is defined to be the most significant bit of the remainder and C_6 the least significant bit of the remainder.

6.1.3.2 *Encoding procedure*

The CRC bit positions are initially set at 0 i.e.:

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = 0$$

The frame is then acted upon by the multiplication/division process referred to above in § 6.1.3.1.

The remainder resulting from the multiplication/division process is stored ready for insertion into the respective CRC locations of the next frame.

Note — These CRC bits do not affect the computation of the CRC bits in the next frame since the corresponding locations are set to 0 before the computation.

6.1.3.3 *Decoding procedure*

A received frame is acted upon by the multiplication/division process, referred to above in § 6.1.3.1, after having its CRC bits extracted and replaced by 0s.

The remainder resulting from this multiplication/division process is then stored and subsequently compared on a bit by bit basis with the CRC received in the next frame.

If the decoder-calculated remainder exactly corresponds to the CRC bits sent from the encoder, it is assumed that the checked frame is error free.

6.1.3.4 *Action on bit E*

Bit E of frame *N* is set to 1 in the transmitting direction if bits C_1 to C_6 detected in the most recent frame at the opposite end have been found in error (at least one bit in error). If no errors, E is set to 0.

6.1.4 *Signalling*

The use of channel time slots 67 to 70 is recommended for either common channel or channel-associated signalling as required. The detailed requirements for the organization of particular signalling systems will be included in the specifications for those signalling systems.

6.1.4.1 *Common channel signalling*

64 kbit/s channel time slots 67 to 70 may be used for common channel signalling in a descending order of priority up to a rate of 64 kbit/s. The method of obtaining signal alignment will form part of the particular common channel signalling specification.

6.1.4.2 *Channel associated signalling*

The recommended arrangement for the use of the 64 kbit/s capacity in each 64 kbit/s channel time slot 67 to 70 for channel associated signalling is as follows:

6.1.4.2.1 *Multiframe structure*

A multiframe for each 64 kbit/s bit-stream comprises 16 consecutive frames (whose structure is given in § 6.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of channel time slots 67 to 70 in frame 0.

6.1.4.2.2 *Allocation of 64 kbit/s channel time slots 67 to 70*

When 64 kbit/s channel time slots 67 to 70 are used for channel associated signalling, the 64 kbit/s capacity of each of the four 64 kbit/s channel time slots is sub-multiplexed into lower rate signalling channels using the multiframe alignment signal as a reference. Details of the bit allocation are given in Table 10/G.704.

6.2 *Interface at 8448 kbit/s carrying other channels than 64 kbit/s*

For further study.

Blanc

H.T. [T11.704]

TABLE 10/G.704

Bit allocation of 64 kbit/s channel time slots 67 to 70

{ 64 kbit/s channel time slot Frame }	67	68	69	70			
0	0000*xyxx*	0000*xyxx*	0000*xyxx*	0000*xyxx*			
1	*abcd* Channel 1	*abcd* Channel 16	*abcd* Channel 31	*abcd* Channel 46	*abcd* Channel 61	*abcd* Channel 76	*abcd* Channel 91	*abcd* Channel 106
15	*abcd* Channel 15	*abcd* Channel 30	*abcd* Channel 45	*abcd* Channel 60	*abcd* Channel 75	*abcd* Channel 90	*abcd* Channel 105	*abcd* Channel 120

Note 1 — Channel numbers refer to telephone channel numbers. Refer to § 6.1.2.1 for the assignment of 64 kbit/s channel time slots to the telephone channels.

Note 2 — This bit allocation provides four 500-bit/s signalling channels designated a, b, c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the PCM transmission system, will not exceed ± | ms.

Note 3 — When bits b, c or d are not used they should have the values: b = 1, c = 0, d = 1.

It is recommended the the com bination 0000 of bits *a* , *b* , *c* and *d* should not be used for signalling purposes for channels 1-15, 31-45, 61-75 and 91-125.

Note 4 — x = spare bit, to be set to 1 if not used. y = bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in an alarm condition, set to 1.

Tableau 10/G.704 [T11.704], p. 14

ANNEX A

(to Recommendation G.704)

Examples of CRC implementations using shift registers

A.1 *CRC-6 procedure for interface at 1544 kbit/s* | (Reference: § 2.1.3.1.2)

See Figure A-1/G.704.

Input I to the shift register: CMB *N* with F bits set to 1.

Generator polynomial of the shift register: $x^6 + x + 1$.

Figure A-1/G.704, p.

At I, the CMB is fed serially (i.e. bit by bit) into the circuit, starting with bit number 1 of the multiframe (see Table 1/G.704). When the last bit of the CMB (i.e. bit number 4632 within the multiframe has been fed into the shift register, the CRC bits e_1 to e_6 are available at the outputs 1 to 6. (Output 1 provides the most significant bit, e_1, and output 6 the least significant bit, e_6). Bits e_1 to e_6 are transmitted in the next CMB (c.f. Table 1/G.704).

Note — The outputs (1 to 6) of the shift register stages are reset to 0 after each CMB.

A.2 *CRC-5 procedure for interface at 6312 kbit/s* | (Reference: § 2.2.3.2)

Input I to the shift register: CMB *N* .

Generator polynomial of the shift register: $x^5 + x^4 + x^2 + 1$.

Figure A-2/G.704, p.

At I, the CMB is fed serially (i.e. bit by bit) into the circuit, starting with bit number 1 of frame number 1 (see Table 3/G.704). When the last bit of the CMB (i.e. bit number 784 of frame number 4) has been fed into the the shift register, the CRC bits e_1 to e_5 are available at the outputs 1 to 5. (Output 1 provides the most significant bit, e_1, and output 5 the least significant bit, e_5). Bits e_1 to e_5 are transmitted in the corresponding multiframe (see Table 3/G.704).

Note — The outputs (1 to 5) of the shift register stages are reset to 0 after each CMB.

A.3 *CRC-4 procedure for interface at 2048kbit/s* | (Reference: § 2.3.3.5)

See Figure A-3/G.704.

Input I to the shift register: SMF (*N*) with C_1, C_2, C_3, C_4 set to 0.

Generator polynomial of the shift register: $x^4 + x + 1$.

Figure A-3/G.704, p.

At I, the SMF is fed serially (i.e. bit by bit) into the circuit, starting with bit $C_1 = 0$ (see Table 4b/G.704). When the last bit of the SMF (i.e. bit number 256 of frame number 7, respectively of frame number 15) has been fed into the shift register, the CRC bits C_1 to C_4 are available at the outputs 1 to 4. (Output 1 provides the most significant bit, C_1, and output 4 the least significant bit, C_4). Bits C_1 to C_4 are transmitted in the next SMF, i.e. SMF(*N* +1).

Note — The outputs (1 to 4) of the shift register stages are reset to 0 after each SMF.

Recommendation G.705

CHARACTERISTICS REQUIRED TO TERMINATE DIGITAL LINKS ON A DIGITAL EXCHANGE

(Malaga-Torremolinos, 1984)

This Recommendation defines interface conditions and fundamental functions of digital exchange terminal equipments used to terminate digital paths. The multiplex structures are compatible with those described in Recommendation G.704, and are applicable to digital paths which connect PCM multiplex equipments to exchanges and to digital paths which interconnect digital exchanges. The locations of these interfaces are described in Recommendations Q.502 and Q.512 for digital transit and digital local exchanges.

The digital exchange terminal is a synchronous equipment which has a frame aligner circuit. In order to meet the network performance objectives of Recommendation G.822, the digital exchange terminal should fulfil the synchronization performance as described below.

1 1544 kbit/s digital path

1.1 *General characteristics*

1.1.1 *Bit rate*

The nominal bit rate is 1544 kbit/s.

Note — The tolerance on this bit rate should be further studied and specified.

1.1.2 *Timing signal*

It should be possible to derive the transmitting timing signal from an external source as specified below.

Note — For PCM multiplex equipment at the remote end, the timing signal will be derived from the incoming signal at the receive end.

1.1.2.1 *Timing in a non-synchronized network*

For a digital exchange the transmitting timing signal will be derived from an office clock.

1.1.2.2 *Timing in a synchronized network*

In case of synchronous operation of the network, a network synchronization system will maintain the signal or clocks within agreed timing limits.

1.1.3 *Interfaces*

Refer to § 2 of Recommendation G.703. No interface internal to the switch will be recommended.

1.1.4 *Transmission performance*

Transmission performance of the digital path should be the same as that for 1544 kbit/s digital paths between primary PCM multiplex equipment.

1.2 *Frame strusture*

Refer to § 3.1 of Recommendation G.704.

1.3 *Synchronization performances*

1.3.1 *Wander at the input*

Refer to § 4 of Recommendation G.824.

1.3.2 *Jitter at the input*

Refer to § 4 of Recommendation G.824.

1.3.3 *Jitter at the output*

Jitter at the output is under study.

1.3.4 *Slips*

Refer to §§ 3 and 4 of Recommendation G.822.

1.3.5 *Forms of frame aligner*

Refer to § 8 of Recommendation G.811.

2 6312 kbit/s digital path

2.1 *General characteristics*

2.1.1 *Bit rate*

The nominal bit rate is 6312 kbit/s.

Note — The tolerance on this bit rate should be further studied and specified.

2.1.2 *Timing signal*

It should be possible to derive the transmitting timing signal from an external source as specified below.

Note — For PCM multiplex equipment at the remote end, the timing signal will be derived from the incoming signal at the receive end.

2.1.2.1 *Timing in a non-synchronized network*

For a digital exchange the transmitting timing signal will be derived from an office clock.

2.1.2.2 *Timing in a synchronized network*

In case of synchronous operation of the network, a network synchronization system will maintain the signal or clocks within agreed timing limits.

2.1.3 *Interfaces*

Refer to § 3 of Recommendation G.703. No interface internal to the switch will be recommended.

2.1.4 *Transmission performance*

Transmission performance of the digital path should be the same as that for 6312 kbit/s digital paths between primary PCM multiplex equipment.

2.2 *Frame structure*

Refer to § 3.2 of Recommendation G.704.

2.3 *Synchronization performances*

2.3.1 *Wander at the input*

Refer to § 4 of Recommendation G.824.

2.3.2 *Jitter at the input*

Refer to § 4 of Recommendation G.824.

2.3.3 *Jitter at the output*

Jitter at the output is under study.

2.3.4 *Slips*

Refer to §§ 3 and 4 of Recommendation G.822.

2.3.5 *Forms of frame aligner*

Refer to § 8 of Recommendation G.811.

3 2048 kbit/s digital path

3.1 *General characteristics*

3.1.1 *Bit rate*

The nominal bit rate is 2048 kbit/s. This rate will be controlled to within at least ± | 0 parts per million (ppm) at the transmitting end for each direction of transmission.

3.1.2 *Timing signal*

The timing signal is a 2048 kHz signal from which the bit rate is derived.

3.1.2.1 *Timing in a non-synchronized network*

For a PCM multiplex equipment, the timing signal will be derived from the incoming timing signal at the receive side. For a digital exchange, the transmitting timing signal will be derived from a clock within the digital exchange.

3.1.2.2 *Timing in a synchronized network*

In case of synchronous operation of the network, a network synchronization system will maintain the timing signal or clocks within agreed timing limits.

3.1.3 *Interfaces*

Refer to § 6 of Recommendation G.703. No interface, internal to the switch, will be recommended.

3.1.4 *Transmission performance*

The transmission performance of the digital path will be the same as that for 2048 kbit/s digital paths between primary PCM multiplex equipments.

3.2 *Frame structure*

Refer to § 3.3 of Recommendation G.704.

Where more signalling capacity is required between exchanges, additional time slots may be utilized for common channel signalling. They should be selected from the slots allocated in PCM multiplexes for data purposes. On routes between exchanges comprising more than one 2048-kbit/s digital path, it may be possible to provide an adequate signalling capacity without using time slot 16 of all systems on the route. In these circumstances time slot 16 in those systems not carrying signalling can be allocated to speech or other services. Time slot 0 is reserved for frame alignment, alarms and network synchronization information and should not be used for signalling or speech purposes.

3.3 *Synchronization performances*

3.3.1 *Wander at the input*

Refer to § 3 of Recommendation G.823.

3.3.2 *Jitter at the input*

Refer to § 3 of Recommendation G.823.

3.3.3 *Jitter at the output*

Jitter at the output is under study.

3.3.4 *Slips*

Refer to §§ 3 and 4 of Recommendation G.822.

3.3.5 *Forms of frame aligner*

Refer to § 8 of Recommendation G.811.

4 8448 kbit/s digital path

4.1 *General characteristics*

4.1.1 *Bit rate*

The nominal bit rate is 8448 kbit/s. This rate will be controlled to within at least ± | 0 parts per million at the transmitting end for each direction of transmission.

4.1.2 *Timing signal*

The timing signal is an 8448 kHz signal from which the bit rate is derived.

4.1.2.1 *Timing in a non-synchronous network*

For a PCM multiplex equipment, the timing signal will be derived from the incoming timing signal at the receive side. For a digital exchange, the transmitting timing will be derived from a clock within the digital exchange.

4.1.2.2 *Timing in a synchronous network*

In case of synchronous operation of the network, a network synchronization system will maintain the timing signal or clocks within agreed timing limits.

4.1.3 *Interfaces*

Refer to § 7 of Recommendation G.703. No interface, internal to the switch, will be recommended.

4.1.4 *Transmission performance*

The transmission performance of the digital path will be the same as that for 8448 kbit/s digital paths between secondary PCM and/or digital multiplex equipments.

4.2 *Frame structure*

Refer to § 3.4 of Recommendation G.704.

Where signalling capacity is required between exchanges, time-slots 67, 68, 69 and 70 may be utilized for common channel signalling in this order of descending priority. Those channels not used for common channel signalling can be used for speech or other purposes.

4.3 *Synchronization performance*

4.3.1 *Wander at the input*

Refer to § 3 of Recommendation G.823.

4.3.2 *Jitter at the input*

Refer to § 3 of Recommendation G.823.

4.3.3 *Jitter at the output*

Jitter at the output is under study.

4.3.4 *Slips*

Refer to §§ 3 and 4 of Recommendation G.822.

4.3.5 *Forms of frame aligner*

Refer to § 8 of Recommendation G.811.

Recommendation G.706

FRAME ALIGNMENT AND CYCLIC REDUNDANCY CHECK (CRC) PROCEDURES RELATING TO BASIC FRAME STRUCTURES DEFINED IN RECOMMENDATION G.704

(Melbourne, 1988)

1 General

This Recommendation relates to equipment which receives signals with basic frame structures as defined in Recommendation G.704. It defines the frame alignment, the cyclic redundancy check (CRC) multiframe alignment and CRC bit error monitoring procedures to be used by such equipment. Annex A contains background information about the use of the CRC procedures and their limitations.

2 Frame alignment and CRC procedures at l544 kbit/s interface

2.1 *Loss and recovery of frame alignment*

There are two alternative multiframe structures at the 1544 kbit/s interface:

a) 24-frame multiframe, and

b) 12-frame multiframe.

2.1.1 *Loss of frame alignment*

The frame alignment signal should be monitored to determine if frame alignment has been lost. Loss of frame alignment should be detected within 12 ms. Loss of frame alignment must be confirmed over several frames to avoid the unnecessary initiation of the frame alignment recovery procedure due to transmission bit errors. The frame alignment recovery procedure should commence immediately once loss of frame alignment has been confirmed.

Note — For the 12-frame multiframe described in Recommendation G.704, loss of multiframe alignment is deemed to occur when loss of frame alignment occurs.

2.1.2 *Recovery of frame alignment*

2.1.2.1 *Frame alignment recovery time*

The frame alignment recovery time is specified in terms of the maximum average reframe time in the absence of errors. The maximum average reframe time is the average time to reframe when the maximum number of bit positions must be examined for locating the frame alignment signal.

a) *24-frame multiframe*

The maximum average reframe time should not exceed 15 ms.

Note — Some existing designs of equipment were designed to a limit of 50 ms.

b) *12-frame multiframe*

The maximum average reframe time should not exceed 50 ms.

Note — These times do not include the time required for the CRC procedure for false frame alignment verification defined in § 2.2.2.

2.1.2.2 *Strategy for frame alignment recovery*

a) *24-frame multiframe*

Frame alignment should be recovered by detecting the valid frame alignment signal. When the CRC-6 code is utilized for error performance monitoring (see § 2.2.3), the CRC-6 information may be coupled with the framing algorithm to ensure that a valid frame alignment signal contained within the 24 F-bits is the only pattern onto which the reframe circuit can permanently lock. This procedure is illustrated in Figure 1/G.706.

b) *12-frame multiframe*

Overall frame alignment should be recovered by way of simultaneous detection of the frame alignment signal and the multiframe alignment signal, or of frame alignment followed by multiframe alignment.

Figure 1/G.706, p. 18

2.2 *CRC bit monitoring*

Error monitoring by CRC-6 assumes a signal quality sufficient for frame alignment to be established so that CRC-6 bits can be correctly accessed.

2.2.1 *Monitoring procedure*

i) A received CRC Message Block (CMB) is acted upon by the multiplicationB/Fdivision process defined in Recommendation G.704 after having its F-bits replaced by binary 1s.

ii) The remainder resulting from the division process is then stored and compared on a bit-by-bit basis with the CRC bits received in the next CMB.

iii) If the remainder exactly corresponds to the CRC bits contained in the next CMB of the received signal, it is assumed that the checked CMB is error-free.

2.2.2 *Monitoring for false frame alignment* (see § A.1.1)

In the case of the 24-frame multiframe, when the CRC-6 code is utilized for error performance monitoring, it may also be used to provide immunity against spurious frame alignment signals. The procedure described in § 2.1.2.2 a) should be followed.

2.2.3 *Error performance monitoring using CRC-6* (see § A.1.2)

For the purpose of error performance monitoring, it should be possible to obtain indications of each CRC message block which is received in error. The consequent error information should be used in accordance with the requirements to be defined in respective equipment Recommendations.

3 **Frame alignment and CRC procedures at 6312 kbitB/Fs interface**

3.1 *Loss and recovery of frame alignment*

For the 6312 kbitB/Fs hierarchical level, the term ‘‘frame alignment’’ is synonymous with ‘‘multiframe alignment’’. The last five bits of the 789-bit frame are designated as the F-bits (see Recommendation G.704) and are time-shared as a frame alignment signal and for other purposes.

3.1.1 *Loss of frame alignment*

The frame alignment signal should be monitored to determine if frame alignment has been lost. The loss of frame alignment is declared when seven consecutive incorrect frame alignment signals have been received.

The recovery of frame alignment procedure should start immediately once loss of frame alignment has been confirmed.

3.1.2 *Recovery of frame alignment*

3.1.2.1 *Frame alignment recovery time*

The frame alignment recovery time is specified in terms of the maximum average reframe time in the absence of errors. The maximum average reframe time is the average time to reframe when the maximum number of bit positions must be examined for locating the frame alignment signal.

The maximum average reframe time should be less than 5 ms.

3.1.2.2 *Strategy for frame alignment recovery*

Frame alignment should be recovered by detecting three consecutive correct frame alignment signals. In addition to this, the CRC-5 code (see § 3.2) should be coupled with the framing algorithm to ensure that a valid frame alignment signal contained within the F-bits is the only pattern onto which the reframe circuit can permanently lock. This procedure is illustrated in Figure 1/G.706.

3.2 *CRC bit monitoring*

Error monitoring by CRC-5 assumes a signal quality sufficient for frame alignment to be established so that the CRC-5 bits can be correctly accessed.

3.2.1 *Monitoring procedure*

i) A received sequence of 3156 serial bits (i.e. 3151 bits of CMB and 5 CRC bits) is divided by the generator polynomial defined in Recommendation G.704.

ii) If the remainder resulting from the division process is 00000, it is assumed that the checked CMB is error-free.

3.2.2 *Monitoring for false frame alignment* (see § A.1.1)

The procedure in § 3.1.2.2 should be followed when the CRC-5 code is used to provide immunity against false frame alignment signal.

Using the CRC-5 code, it should be possible to detect false frame alignment within 1 second and with greater than 0.99 probability. On detection of such an event, a re-search for correct frame alignment should be initiated.

With a random error ratio of 10^{-4}, the mean time between two events of falsely initiating a search for frame alignment due to an excessive number of errored CRC message blocks should be more than one year.

Note 1 — With a random error ratio of approximately 10^{-3}, it is almost impossible to distinguish whether CRC errors are caused by the false frame alignment or by transmission bit errors.

Note 2 — To achieve the probability bounds stated above, one method is to count the errored CRC-5 message blocks with the understanding that a count of 32 consecutive errored CRC-5 blocks indicates false frame alignment.

3.2.3 *Error performance monitoring using CRC-5* (see § A.1.2)

For the purpose of error performance monitoring, it should be possible to obtain indications for each CRC message block which is received in error. The consequent error information should be used in accordance with the requirements to be defined in the respective equipment Recommendations.

4 Frame alignment and CRC procedures at 2048 kbit/s interface

4.1 *Loss and recovery of frame alignment*

4.1.1 *Loss of frame alignment*

Frame alignment will be assumed to have been lost when three consecutive incorrect frame alignment signals have been received.

Note 1 — In addition to the preceding, in order to limit the effect of spurious frame alignment signals, the following procedure may be used:

Frame alignment will be assumed to have been lost when bit 2 in time slot 0 in frames not containing the frame alignment signal has been received with an error on three consecutive occasions.

Note 2 — Loss of frame alignment can also be invoked by an inability to achieve CRC multiframe alignment in accordance with § 4.2, or by exceeding a specified count of errored CRC message blocks as indicated in § 4.3.2.

4.1.2 *Strategy for frame alignment recovery*

Frame alignment will be assumed to have been recovered when the following sequence is detected:

— for the first time, the presence of the correct frame alignment signal;

— the absence of the frame alignment signal in the following frame detected by verifying that bit 2 of the basic frame is a 1;

— for the second time, the presence of the correct frame alignment signal in the next frame.

Note — To avoid the possibility of a state in which no frame alignment can be achieved due to the presence of a spurious frame alignment signal, the following procedure may be used:

When a valid frame alignment signal is detected in frame *n* , a check should be made to ensure that a frame alignment signal does not exist in frame *n* + 1, and also that a frame alignment signal exists in frame *n* + 2. Failure to meet one or both of these requirements should cause a new search to be initiated in frame *n* + 2.

4.2 *CRC multiframe alignment using information in bit 1 of the basic frame*

If a condition of assumed frame alignment has been achieved, CRC multiframe alignment should be deemed to have occurred if at least two valid CRC multiframe alignment signals can be located within 8 ms, the time separating two CRC multiframe alignment signals being 2 ms or a multiple of 2 ms. The search for the CRC multiframe alignment signal should be made only in basic frames not containing the frame alignment signal.

If multiframe alignment cannot be achieved within 8 ms, it should be assumed that frame alignment is due to a spurious frame alignment signal and a re-search for frame alignment should be initiated.

Note 1 — The re-search for frame alignment should be started at a point just after the location of the assumed spurious frame alignment signal. This will usually avoid realignment onto the spurious frame alignment signal.

Note 2 — Consequent actions taken as a result of loss of frame alignment should no longer be applied once frame alignment has been recovered. However, if CRC multiframe alignment cannot be achieved within a time limit in the range of 100 ms to 500 ms, e.g. owing to the CRC procedure not being implemented at the transmitting side, consequent actions should be taken equivalent to those specified for loss of frame alignment.

4.3 *CRC bit monitoring*

If frame and CRC multiframe alignment have been achieved, the monitoring of the CRC bits in each sub-multiframe should commence.

4.3.1 *Monitoring procedure*

i) A received CRC sub-multiframe (SMF) is acted upon by the multiplication/division process defined in Recommendation G.704 after having its CRC bits extracted and replaced by 0s.

ii) The remainder resulting from the division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.

iii) If the remainder exactly corresponds to the CRC bits contained in the next SMF of the received signal, it is assumed that the checked SMF is error-free.

4.3.2 *Monitoring for false frame alignment* (see § A.1.1)

It should be possible to detect a condition of false frame alignment within 1 second and with a probability greater than 0.99. On detection of such an event, a re-search for frame alignment should be initiated.

With a random error ratio of 10$^{\mathrm{D}}$lF261^{3} the probability of falsely initiating a search for frame alignment due to an excessive number of errored CRC blocks should be less than 10$^{\mathrm{D}}$lF261^{4} over a 1 second period.

Figure 2/G.706 shows an illustration of the procedure to be followed in passing from the frame alignment search to error monitoring using CRC.

Note 1 — The re-search for frame alignment should be started at a point just after the location of the assumed spurious frame alignment signal. This will usually avoid realignment onto the spurious frame alignment signal.

Note 2 — To achieve the probability bounds stated above, a preferred threshold count is 915 errored CRC blocks out of 1000, with the understanding that a count of ≥" | 15 errored CRC blocks indicates false frame alignment.

Figure 2/G.706, p.

4.3.3 *Error performance monitoring using CRC-4* (see § A.1.2)

Information on the status of the CRC processing should be made available in two forms:

a) *Direct information*

Every time a CRC block is detected in error, it will be necessary to indicate this condition.

b) *Integrated information*

In consecutive 1 second periods, the number of errored CRC blocks should be made available. This number will be in the range 0 to 1000 (decimal).

5 Frame alignment and CRC procedures at 8448 kbitB/Fs interface

For further study.

ANNEX A

(to Recommendation G.706)

Background information on the use of cyclic

redundancy check (CRC) procedures

A.1 *Reasons for application of CRC*

CRC procedures can be used for both protection against false frame alignment and for bit error monitoring.

A.1.1 *Protection against false frame alignment*

The CRC procedures are used to protect against false frame alignment of receivers of multiplex signals. For example, false frame alignment could occur in an ISDN if a user imitates a frame alignment signal in his non-voice terminal. However, since a user is not controlling the composition of a multiplex frame, the addition of CRC bits, and evaluation of these bits in the receiver, leads to detection of the false frame alignment.

A.1.2 *Bit error monitoring*

The CRC procedure is also used for improved bit error ratio monitoring if low values of error ratio (e.g. 10^{-6}) are to be considered. CRC monitoring (like monitoring of the frame alignment signal) takes account of the entire digital link between the source and sink of a multiplex signal, as opposed to code violation monitoring (e.g. monitoring of AMI, HDB3 or B8ZS violations) which concerns only the digital line section nearest to the receiver, or in many cases only an interface line [e.g. between a digital multiplexer and an Exchange Terminal (ET)].

A.2 *Limitations of CRC procedures*

A.2.1 *Probability of undetected bit errors*

It can be estimated [1] that for CRC-n, and long message/check blocks, the probability that an error remains undetected approaches 2^{-n} even with a high bit error ratio; with a low bit error ratio, the probability is lower. The resulting inaccuracy (at most, with CRC-4, about 6% of blocks with undetected errors; similarly, with CRC-6, 1.6%) is tolerable for the required purpose.

A.2.2 *Limitation of application to bit error ratio measurement*

The CRC monitoring procedure is not well suited to measure values of bit error ratio that are so high that on average every message/check block contains at least one bit error (i.e. for BER = 10^{-3} or higher).

Reference

[1] LEUNG, C. and WITZKE, K.A. — A comparison of some error detecting CRC code standards. *IEEE Trans* . Vol. COM-33, pp. 996-998, 1985.

Recommendation G.707

SYNCHRONOUS DIGITAL HIERARCHY BIT RATES

(Melbourne, 1988)

The CCITT,

considering

(a) that Recommendation G.702 specifies a number of digital hierarchy bit rates for 1544 kbitB/Fs and 2048 kbit/s based digital networks;

(b) that the various hierarchy levels specified in Recommendation G.702 are interconnected by means of digital multiplexing employing justification methods;

(c) that synchronous digital multiplexing and a related synchronous digital hierarchy offer advantages such as:

— simplified multiplexingB/Fdemultiplexing techniques;

— direct access to lower speed tributaries, without need to multiplexB/Fdemultiplex the entire high speed signal;

— enhanced Operations, Administration and Maintenance (OAM) capabilities;

— easy growth to higher bit rates in step with the evolution of transmission technology;

(d) that the synchronous digital hierarchy rates need to be chosen such that they allow the transport of digital signals:

— at hierarchical bit rates as specified in Recommendation G.702;

— at broadband channel bit rates;

(e) that Recommendation G.708 specifies the Network Node Interface (NNI) for the synchronous digital hierarchy;

(f) that Recommendation G.709 specifies the synchronous multiplexing structure;

(g) that Recommendations G.707, G.708 and G.709 form a coherent set of specifications for the synchronous digital hierarchy and NNI.

recommends

(1) that the first level of the synchronous digital hierarchy shall be 155 | 20 kbit/s;

(2) that higher synchronous digital hierarchy bit rates shall be obtained as integer multiples of the first level bit rate;

(3) that higher synchronous digital hierachy levels should be denoted by the corresponding multiplication factor of the first level rate;

(4) that the following bit rates should constitute the synchronous digital hierarchy:

H.T. [T1.707]
TABLE 1/G.707

{ Synchronous digital hierarchy level }	Hierarchical bit rate kbit/s
1	155 | 20
4	622 | 80

Note — The specification of higher synchronous digital hierarchy levels requires further study. Possible candidates are:

Level	*Bit rate*
8 12 16	{
1 | 44 | 60 kbit/s	
1 | 66 | 40 kbit/s	
2 | 88 | 20 kbit/s	
}	

Tableau 1/G.707 [T1.707], p. 20

Blanc